

User Manual

AIMB-506

Intel® /Core™ i7/i5/i3 /Pentium/ Celeron LGA1151 MicroATX with VGA/DVI/DP/eDP (LVDS), 14 COM, Dual LAN, DDR4, PCle x 16, PCle x 1, PCl x 2 and SATAIII



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Caution! There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

CPU Compatibility

CPU Family	Core Number	Power	Freq(GHz)	Mfg-Tech	Smart cach (L3)	Package Type	Result
Intel i7-9700E	8	65W	2.6G	14nm	12MB	LGA1511	Pass
Intel i7-9700TE	8	35W	1.8G	14nm	12MB	LGA1511	Pass
Intel i7-8700	6	65W	3.2G	14nm	12MB	LGA1511	Pass
Intel i7-8700T	6	35W	2.4G	14nm	12MB	LGA1511	Pass
Intel i5-9500E	6	65W	3.0G	14nm	9MB	LGA1511	Pass
Intel i5-9500TE	6	35W	2.2G	14nm	9MB	LGA1511	Pass
Intel i5-8500	6	65W	3.0G	14nm	9MB	LGA1511	Pass
Intel i5-8500T	6	35W	2.1G	14nm	9MB	LGA1511	Pass
Intel i3-9100E	4	65W	3.1G	14nm	6MB	LGA1511	Pass
Intel i3-9100TE	4	35W	2.2G	14nm	6MB	LGA1511	Pass
Intel i3-8100	4	65W	3.6G	14nm	6MB	LGA1511	Pass
Intel i3-8100T	4	35W	3.1G	14nm	6MB	LGA1511	Pass
Intel Pentium® Processor G5400	2	58W	3.7G	14nm	4MB	LGA1511	Pass
Intel Pentium® Processor G5400T	2	35W	3.1G	14nm	4MB	LGA1511	Pass
Intel Celeron® Processor G4900	2	54W	3.1G	14nm	2MB	LGA1511	Pass
Intel Celeron® Processor G4900T	2	35W	2.9G	14nm	2MB	LGA1511	Pass

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- 4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
- 5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Ordering Information

Part Number	РСН	Memory	VGA	DVI		-	USB 3.0/2.0	сом	SATA					PCI slot	АМР
AIMB-506F-00A1E	H310	Non ECC	1	1	1	1/(1)	8/12	14	3	2	1	1	1	2	1
AIMB-506G2-00A1E	H310	Non ECC	1	1	1	(1)/(1)	4/8	10	3	2	1	1	1	2	1
AIMB-506GL-00A1E	H310	Non ECC	1	1	(1)	-/-	4/4	2	3	1	1	1	0	0	(1)

^{*()} BOM options available on MP version

Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-506 Intel LGA 1151 Core i7/i5/i3 /Pentium/Celeron Micro ATX Motherboard
- 2 x SATA HDD cable
- 1 x COM 1 to 2 cable
- 1 x COM 1 to 4 cable
- 1 x I/O port bracket
- 1 x Startup manual
- 1 x Warranty card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-506 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-506, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

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Chapter

General Information

1.1 Introduction

AIMB-506 is designed with the Intel H310 for industrial applications that require both high-performance computing and enhanced power management capabilities. The motherboard supports 8th /9th Intel® Core™ i7/i5/i3 embedded processors up to 8 MB L3 cache and DDR4 2666 MHz up to 64GB, per slot up to 32GB. Multiple I/O connectivity of 14 serial ports, 12 USB 2.0, 8 USB 3.0, dual GbE LAN, and 3 SATA III ports are offered.

1.2 Features

- Multiple I/O connectivity: Dual GbE LAN via PCle x1 bus, 1 x PCle x16 slot (Gen 3), 1 x PCle x1 slot (Gen 2), 1 x PCl, 12 x USB 2.0 ports and 8 x USB 3.0 ports.
- Standard Micro ATX form factor with industrial features: The AIMB-506 is a full-featured Micro ATX motherboard with balanced expendability and performance.
- Wide selection of storage devices: SATAIII HDD, customers benefit from the flexibility of using the most suitable storage device for larger capacity.
- **Optimized integrated graphics solution:** With Intel® Flexible Display Interface, it supports versatile display options and 32-bit 3D graphics engine.

1.3 Specifications

1.3.1 System

- CPU: Intel 8th/9th generation Core i7/i5/i3 /Pentium/Celeron processor
- BIOS: AMI EFI 128 Mbit SPI BIOS
- System chipset: Intel® H310
- SATA hard disk drive interface: Three on-board SATA connectors with data transmission rates up to 600 MB

1.3.2 Memory

- RAM: Up to 64 GB in 2 slots 288-pin DIMM sockets. Supports dual-channel DDR4 2666 MHz SDRAM.
 - AIMB-506G2 & AIMB-506L supports non-ECC unbuffered DIMMs and do not support any memory configuration that mixes non-ECC with ECC unbuffered DIMMs.

Note! A 32-bit OS may not fully detect 4GB of RAM when 4 GB is installed.



1.3.3 Input/Output

- PCle slot: 1 PCle x16 expansion slot, 1 PCle x 1 expansion slot, 2 PCl
- **Serial port**: Fourteen serial ports, COM3 and COM7 are RS-232/422/485 with hardware auto-flow control and the rest are RS-232.
- Keyboard and PS/2 mouse connector: Two 6-pin mini-DIN connectors are located on the mounting bracket for easy connection to PS/2 keyboard and mouse
- **USB port:** Supports up to 12 USB 2.0 ports with transmission rates up to 480 Mbps and 8 USB 3.0 ports with transmission rates up to 5 Gbps.
- **GPIO:** AIMB-506 supports 16-bit GPIO from super I/O for general purpose control applications.

1.3.4 Graphics

- Controller: Intel® HD Graphics
- **Display memory:** 1 GB maximum shared memory with 2GB and above system memory installed
- **DVI:** Supports DVI up to resolution 1920 x 1200 @ 60Hz refresh rate
- **VGA:** Supports VGA up to resolution 1920 x 1200 @ 60Hz refresh rate
- **Display Port**: Supports max resolution 4096 x 2304 @60Hz
- eDP: Supports max resolution 3840 x 2160 @ 60Hz
- LVDS (BOM option eDP): Support max resolution 1920 x 1200
- Dual Display: VGA+eDP/LVDS, VGA+DVI, eDP/LVDS+ DVI, LVDS + DP, DP+DVI, eDP/LVDS+DP

1.3.5 Ethernet LAN

- Supports dual 10/100/1000 Mbps Ethernet port (s) via PCI Express x1 bus which provides 500 MB/s data transmission rate
- Controller: LAN1: Realtek 8111G; LAN2:Intel Realtek 8111G

1.3.6 Industrial features

■ Watchdog timer: Can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels)

1.3.7 Mechanical and Environmental Specifications

■ Operating temperature: 0 ~ 60° C (32 ~ 140° F, Depending on CPU)

■ Storage temperature: -40 ~ 85° C (-40 ~ 185° F)

■ **Humidity**: 5 ~ 95% non-condensing

Power supply voltage: +3.3 V, +5 V, +12 V, -12 V, 5 Vsb, 12V_4P

Power consumption:

LAG1151 Core i7-9700E 2.6 GHz, 12MB L3 Cache, 2pcs 16GB DDR4 2666MHz memory

+5 V 3.3 V 12V_4P 5 Vsb -12 V 12V 0.7A 0.78A 3.462A 0.53A 0 A 0.303A

Measure the maximum current value with system under maximum load (CPU: Top speed, RAM & Graphic: Full loading)

■ Board size: 244 mm x 244 mm (9.6" x 9.6")

■ Board weight: 0.365 kg

1.4 Jumpers and Connectors

Connectors on the AIMB-506 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure your system for your application.

The tables below list the function of each of the board jumpers and connectors. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

Table 1.1: Jumpers	
Label	Function
JFP1 (Keyboard Lock and Power LED)	Power LED S3/S4: Fast flash / Slow flash (ATX) System On: ON (ATX/ AT) System Off: OFF (AT) System Off: Slow flash (ATX)
JSETCOM3/7	Serial port: RS232/RS422/RS485 jumper setting
JCMOS1	eDP1 and LVDS power jumper
JLVDS1	Case open connector
JWDT1+JOBS1	Watch dog & beep pin header
JCASEOP_SW1	Case open switch pin header
JLVDS_VCON1	LVDS VESA, JEIDA format selection pin header
JSETCOM1_V1	COM1 voltage selection
JSETCOM2_V2	COM2 voltage selection
PSON1	AT(1-2) / ATX(2-3) (Default 2-3)

Table 1.2: Connecte	ors
Label	Function
LANLED1	Front panel LAN indicator connector
COM12	Serial port 1/2 (RS-232)
COM3/4/5/6	Serial port: COM 3/4/5/6, box header 2 x 20 p Serial port COM3 support RS232/422/485
COM7/8/9/10	Serial port: COM 7/8/9/10, box header 2 x 20 p Serial port COM7 support RS232/422/485
COM11/12/13/14	Serial port: COM 11/12/13/14, box header 2 x 20 p
KBMS1	On board external keyboard and mouse connector
LAN1_USB12	LAN1 & USB12 connector
LAN2_USB34	LAN2 & USB34 connector
USB 5/6/7/8	USB port 5-8
USB 9/10/11/12	USB port 9-12
USB 13/14/15/16/17/18/ 19/20	USB port 13/14/15/16/17/18/19/20 (internal 2 x 10 pin header on board) (optional)
AUDIO1	Line out, Mic IN connector
FPAUDIO1	Front panel audio connector
SPI_CN1	SPI flash programming connector
SATA1-3	Serial III ATA connector
GPIO1	GPIO pin header(SMD pitch=2.0 mm)
ATX12V1 ATX12V2	ATX 12V 4/8 pin Auxiliary power connector
EATXPWR1	ATX power connector
CPUFAN1	CPU FAN connector (4 pin)
SYSFAN1/2/3/4	System FAN power connector (4 pin)
LVDS_EDP1	LVDS/eDP panel header
INV1	EDP/LVDS inverter
VOLT1	Voltage display connector
SPDIF1	Digital audio connector 4 x 1 header pitch =2.54mm
SMBUS1	SMBUS expansion pin header 1 x 4 p
SIM1	SIM card connector
LPC1	Low pin count interface (2x7 pin header)
M2B1	M.2 (B Key /2242)
SP1	Buzzer
SPI1	SPI BIOS flash socket
AMP1	Audio amplifier output connector
JSMB2	SMBus header
JFP2	Power switch/ reset/ external speaker/ SATA HDD LED / SMBus connector
JCASE1	Case open connector

1.5 Board Layout: Jumper and Connector Locations

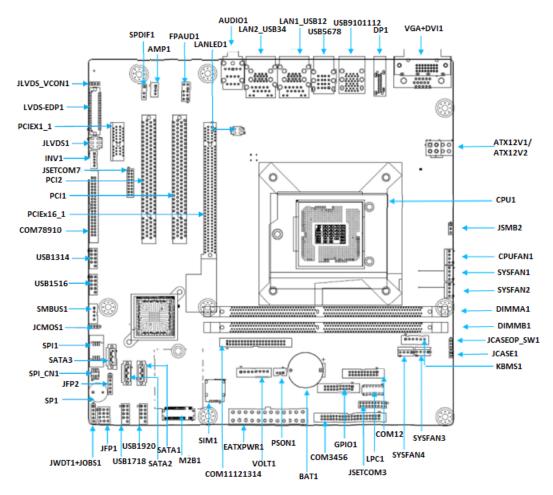


Figure 1.1 Jumper and Connector Locations



Figure 1.2 I/O Connectors

1.6 AIMB-506 Board Diagram

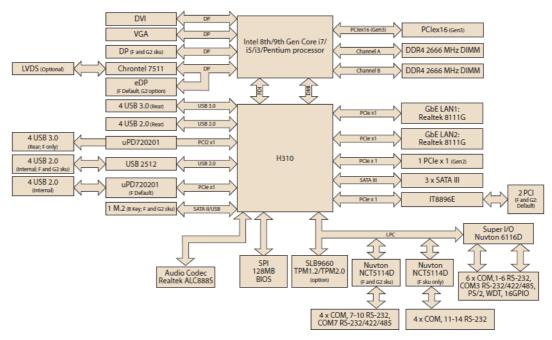


Figure 1.3 AIMB-506 Block Diagram

1.7 **Safety Precautions**



Warning! Always completely disconnect the power cord from chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.



Caution! Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.



Caution! The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Discard used batteries according to manufacturer's instructions.



Caution! There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

1.8 Jumper Settings

This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboards's default settings and your options for each jumper.

1.8.1 How to Set Jumpers

You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" (or turn ON) a jumper, you connect the pins with the clip. To "open" (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

1.8.2 CMOS Clear (JCMOS1)

The AIMB-506 motherboard contains a jumper that can erase CMOS data and reset the system BIOS information. Normally this jumper should be set with pins 1-2 closed. If you want to reset the CMOS data, set JCMOS1 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed. This procedure will reset the CMOS to its default setting.

Table 1.3: JCMOS1						
Function	Jumper Settings					
*Keep CMOS data		1-2 closed				
Clear CMOS data	000	2-3 closed				

^{*} Default

1.8.3 JLVDS1: LVDS Panel Voltage 3.3V/ 5V/ 12V selection

Table 1.4: JLVDS1:	LVDS Panel 3.3 V/5 V/ 12 V Selector
Closed Pins	Result
*JEDP1, 4-6	Jumper for +3.3 V
EDP1, 2-4	Jumper for +5 V
JEDP1, 3-4	Jumper for +12 V
*Default	
Jumper position for +3.3	2 4 6 O O O 1 3 5 2 4 6
Jumper position for +5V	1 3 5
Jumper position for +12\	2 4 6 O O O O O O 1 3 5

1.8.4 PSON1: ATX, AT Mode Selector

Table 1.5: PSON1: ATX, AT Mode Selector					
Closed Pins	Result				
1-2	AT Mode				
2-3*	ATX Mode				
*Default	AT Mode 1-2 closed	1 ATX Mode 2-3 closed			

1.8.5 JWDT1+JOBS1: Watchdog Timer Output, OBS Alarm Option

Table 1.6: JWDT1+JOBS1: Watchdog & Beep Pin Header						
Pin	Pin Name					
1	NC					
2	Watchdog Reset# outp	ut				
3	System Reset input#					
4	SIO Warning Beep out	out				
5	SP1 Buzzer Beep inpu	t .				
Watchdog Timer Output OBS BEEP (4-5) (Defau	` , ` ,	1 2 3 4 5 □ ○ ○ ○ ○ (2 and 3) + (4 and 5)				
Watchdog Timer Disable OSB BEEP (4-5) (Defau	• •	1 2 3 4 5 □ ○ ○ ○ ○ (1 and 3) + (4 and 5)				

1.8.6 JSETCOM3/7: COM3/7 RS232, RS422, RS485 Selection

Table 1.7: C	OM2 RS232, RS	422, RS485 Selectio	n
Pin	Signal	Pin	Signal
1	UART_SIN [2]	2	RXD_RS485
3	UART_SIN [2]	4	RXD_RS422
5	UART_SIN [2]	6	RXD_RS232
7	DCDB	8	SOUT [2]
9	COM2_DCD#	10	COM2_SOUT
11	COM2_TXD485-	12	COM2_RXD485+
13	SIN [B]	14	DTR [B]
15	COM2_SIN	16	COM2_DTR#
17	COM2_TXD485+	18	COM2_RXD485-

	2	4	6	8	10	12	14	16	18	
RS-232 Mode (Default) (5-6) (7-9) (8-10) (13-15) (14-16)	0 0	0 0	•	0	•	0	•	0	0 0	
	1	3	5	7	9	11	13	15	17	
	2	4	6	8	10	12	14	16	18	
RS-422 Mode (3-4) (9-11) (10-12) (15-17) (16-18)	0	•	0	0 0	• •	•	0	0	0	
	1	3	5	7	9	11	13	15	17	
	2	4	6	8	10	12	14	16	18	
RS-485 Mode (1-2) (9-11) (10-12) (15-17) (16-18)	•	00	0	0 0	•	•	0	•	0	
	1	3	5	7	9	11	13	15	17	

1.8.7 LVDS VESA, JEIDA Format Selection Pin Header

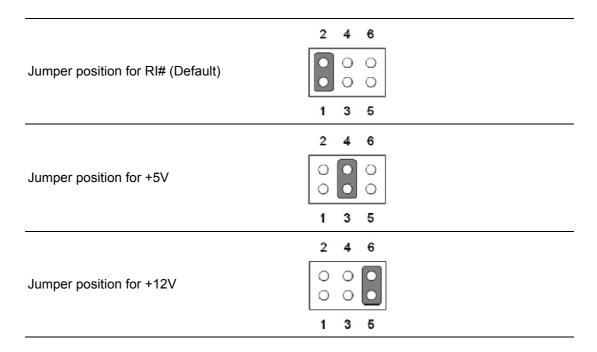
JEIDA mode (HI=+3.3V)

VESA mode (Low=0V) (Default)

1.8.8 JCASEOP_SW1: Case Open Selection Pin Header

Table 1.8: JCASEOP_SW1: Case Open Selection Pin Header					
Closed Pins	Result				
1-2	Normal Mode				
2-3*	Normal Open (Default)				
*Default	1	1			
	Normal Close 1-2 closed	Normal Open (Default) 2-3 closed			

1.8.9 JSETCOM1_V1/JSETCOM2_V2: COM1/COM2_RI# Pin RI# / 5V / 12V



1.9 System Memory

AIMB-506 has four 288-pin memory sockets for 2666 MHz memory modules with maximum capacity of 64 GB (Maximum 32 GB for each DIMM).

1.10 Memory Installation Procedures

To install DIMMs, first make sure the two handles of the DIMM socket are in the "open" position, i.e., the handles lean outward. Slowly slide the DIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the DIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the correct position of the DIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

1.11 Cache Memory

The AIMB-506 supports a CPU with one of the following built-in full speed L3 caches:

12MB for Intel Core i7-9700E/ i7-9700TE

12MB for Intel Core i7-8700/ i7-8700T

9MB for Intel i5-9500E/ i5-9500TE

9MB for Intel i5-8500/ i5-8500T

6MB for Intel i3-9100E/ i3-9100TE

6MB for Intel i3-8100/ i3-8100T

4MB for Intel Pentium G5400/ G5400T

2MB for Intel Celeron G4900/ G4900T

The built-in second-level cache in the processor yields much higher performance than conventional external cache memories.

1.12 Processor Installation

The AIMB-506 is designed for LGA1151, Intel Core i7/Core i5/Core i3/Pentium/Celeron processor.

Chapter

Connecting Peripherals

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 USB Ports (LAN1_USB12/ LAN2_USB34/ USB5678/ USB9101112/ USB13141516/ USB17181920)

The AIMB-506 provides up to 20 USB ports. The USB interface complies with USB Specification Rev 2.0 supporting transmission rates up to 480 Mbps and Rev 3.0 supports transmission rates up to 5 Gbps and is fuse protected. The USB interface can be disabled in the system BIOS setup.

The AIMB-506 is equipped with two high-performance 1000 Mbps Ethernet LAN adapters, both of which are supported by all major network operating systems. The RJ-45 jacks on the rear panel provide convenient LAN connection.

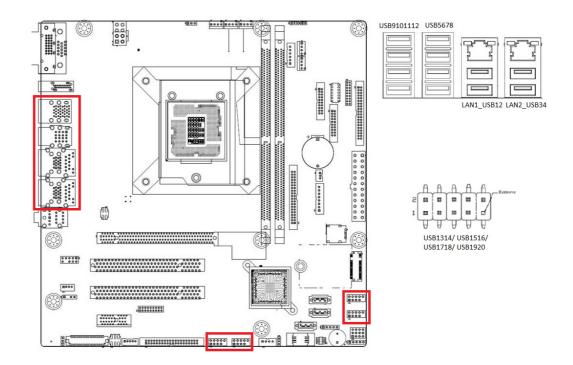
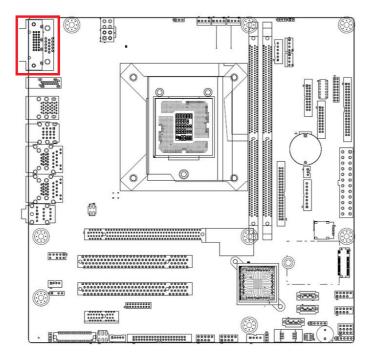


Table 2.1: LAN LED Indicator					
LAN Mode	LAN Indicator				
	LED1 (Right)	off for mal-link; Link (On) / Active (Flash)			
LAN1 Indicator	LED2 (Left)	100 Mbps (On) / 10 Mbps (Off); Color: Orange			
	LED2 (Left)	1000 Mbps (On); Color: Green			
	LED1 (Right)	off for mal-link; Link (On) / Active (Flash)			
LAN2 Indicator	LED2 (Left)	100 Mbps (On) / 10 Mbps (Off); Color: Orange			
	LED2 (Left)	1000 Mbps (On); Color: Green			

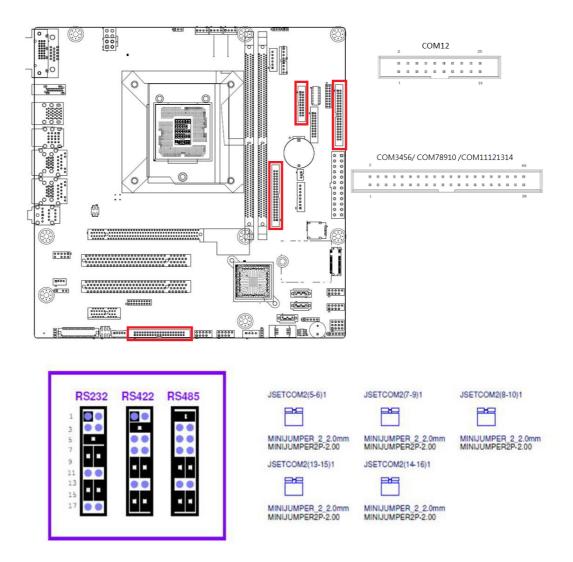
2.3 VGA1/DVI-D Connector (VGA1+DVI 1) Connector





AIMB-506 includes VGA1 and DVI interfaces that can drive conventional VGA1 and DVI displays. Pin assignments for COM1 and DVI connectors are detailed in Appendix B.

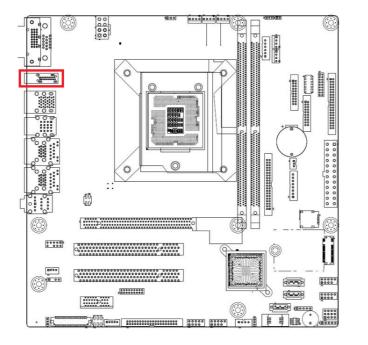
2.4 Serial Ports (COM1~COM14)



AIMB-506 supports 14 serial ports. COM12, COM3-6, COM7-10, COM11-14 support RS-232. JSETCOM3/7 is used to select the RS-232/422/485 mode for COM3/7. These ports can connect to serial devices, such as a mouse or a printer, or to a communications network.

The IRQ and address ranges for both ports are fixed. However, if you want to disable the port or change these parameters later, you can do this in the system BIOS setup. Different devices implement the RS-232 standards in different ways. If you have problems with a serial device, be sure to check the pin assignments for the connector.

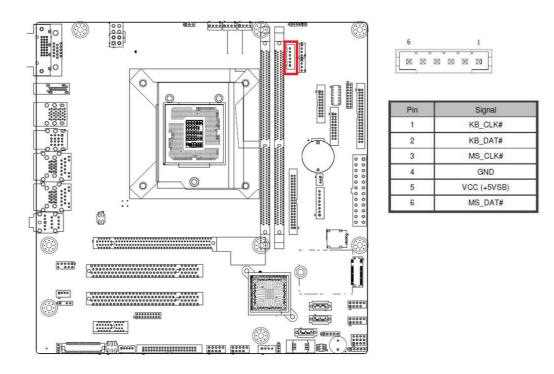
2.5 Display Ports (DP1)





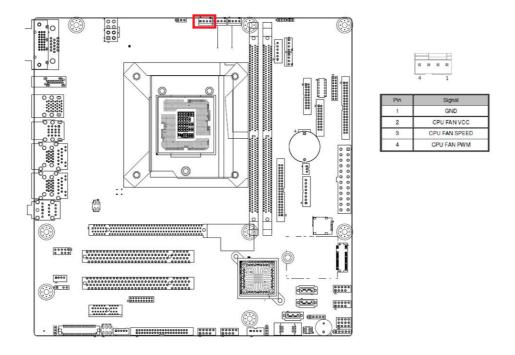
AIMB-506 has one external DP connector to support the Display Port panel. DP max resolution support goes to $4096 \times 2304 \otimes 60 \text{ Hz}$

2.6 PS/2 Keyboard and Mouse Connector (KBMS1)



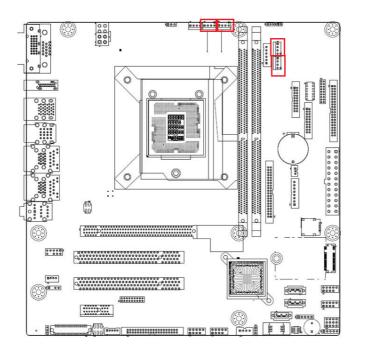
6-pin mini-DIN connectors (KBMS1) support the PS/2 keyboard and PS/2 mouse by a cable P/N 1703060191

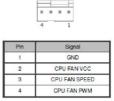
2.7 CPU Fan Connector (CPU_FAN1)



If a fan is used, this connector supports cooling fans of 500 mA (6 W) or less

2.8 System FAN Connector (SYSFAN1/2/3/4)

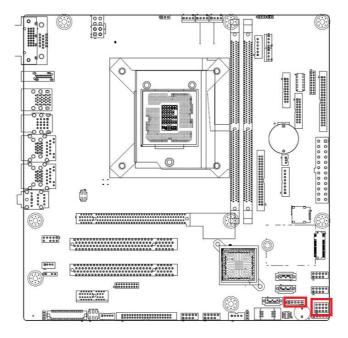


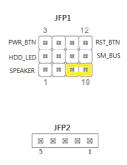


If a fan is used, this connector supports cooling fans of 500 mA (6 W) or less

2.9 Front Panel Connectors (JFP1/JFP2)

There are several headers for monitoring and controlling AIMB-506





2.9.1 ATX Soft Power Switch (JFP1/PWR_SW)

If your computer case is equipped with an ATX power supply, you should connect the power on/off button on your computer case to (JFP1/ PWR_SW), for convenient power on and off.

2.9.2 Reset (JFP1/RESET)

Many computer cases offer the convenience of a reset button. Connect the wire for the reset button.

2.9.3 HDD LED (JFP1/HDDLED)

You can connect an LED to connector (JFP1/HDDLED) to indicate when the HDD is active.

2.9.4 External Speaker (JFP1/SPEAKER)

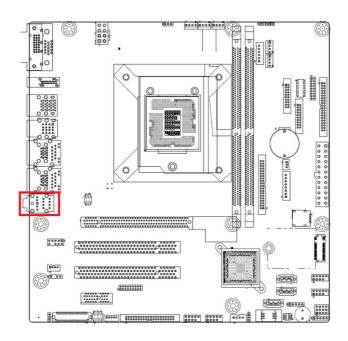
JFP2/SPEAKER is a 4-pin connector for an external speaker. If there is no external speaker, the AIMB-506 provides an onboard buzzer as an alternative. To enable the buzzer, set pins 7 & 10 as closed.

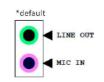
2.9.5 Power LED and Keyboard Lock Connector (JFP2/PWR_LED & **KEY LOCK)**

(JFP2/PWR LED & KEY LOCK) is a 5-pin connector for the power on LED and Key Lock function. Refer to Appendix B for detailed information on the pin assignments. The Power LED cable should be connected to pin 1-3. The key lock button cable should be connected to pin 4-5. There are 3 modes for the power supply connection. The first is "ATX power mode"; the system turns on/off by a momentary power button. The second is "AT Power Mode"; the system turns on/off via the power supply switch. The third is another "AT Power Mode" which makes use of the front panel power switch. The power LED status is indicated in the following table:

Table 2.2: ATX Power Supply LED Status (No Support for AT Power)						
Power Mode	LED (ATX Power Mode) (On/off by momentary button)	LED (AT Power Mode) (On/off by switching power supply)	LED (AT Power Mode) (On/off by front panel switch)			
PSON1 (on back plane) jumper setting	Pins 2-3 closed	Pins 1-2 closed	Connect pins 1 & 2 to panel switch via cable			
System On	On	On	On			
System Off	Off (Windows 7) Slow Flashes (Window 8)	Off	Off			
S3	Fast flashes	N/A	N/A			
S4	Slow flashes	N/A	N/A			

2.10 Line Out, Mic In Connector (AUDIO1)

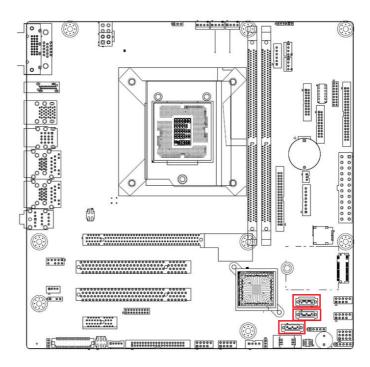




Note! Line out supports 6W AMP out by default.

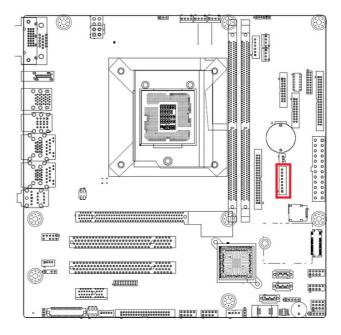


2.11 Serial ATA Interface (SATA1 ~ SATA3)



AIMB-506 features a high performance Serial ATA III interface (up to 600 MB/s) which eases hard drive cabling with thin, space-saving cables

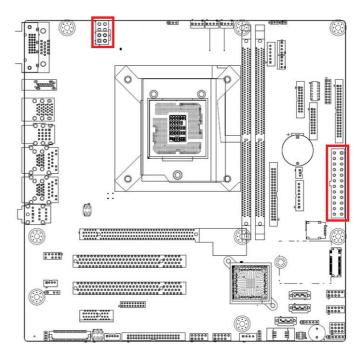
2.12 8-pin Alarm Board Connector (VOLT1)



VOLT1 connects to the alarm board on the chassis. These alarm boards give warnings if a power supply or fan fails, or if the chassis overheats.

2.13 ATX Power Connector (EATXPWR1, ATX12V2)

This connector are for an ATX Micro-Fit power supply. The plugs from the power supply are designed to fit these connectors in only one direction. Determine the proper orientation and push down firmly until the connectors mate completely.



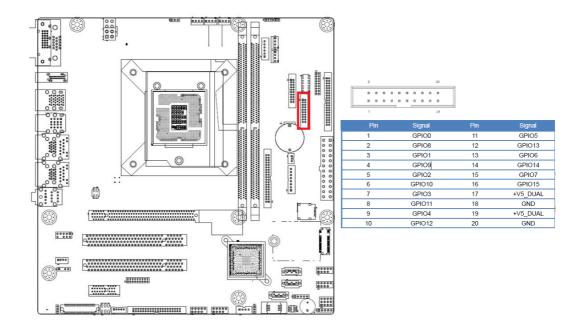
Note!

 Please connect the ATX12V2 connector with the PSU ATX 12V 4pin connector.

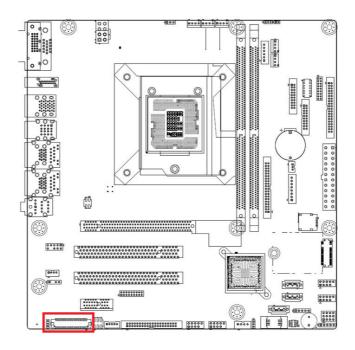


2. For a fully configured system, we recommend that you use a power supply unit (PSU) that complies with ATX 12 V Specification 2.0 (or later version) and provides a minimum power of 180 W.

2.14 General Purpose I/O Connector (GPIO1)



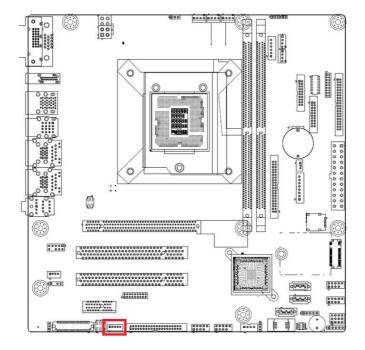
2.15 eDP/LVDS Connector (eDP1/LVDS)

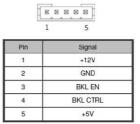


Note! LVDS is BOM option with eDP.

Only G2 and F Sku default with eDP connector.

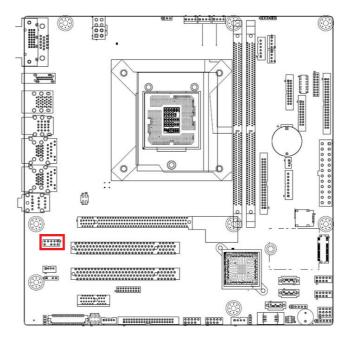
2.16 EDP Backlight Inverter(INV1)





2.17 Front Panel Audio Connector (FPAUD1)

This connector is for a chassis-mounted front panel audio I/O module that supports either HD Audio or legacy AC'97 (optional) audio standard. Connect this connector with the front panel audio I/O module cable.



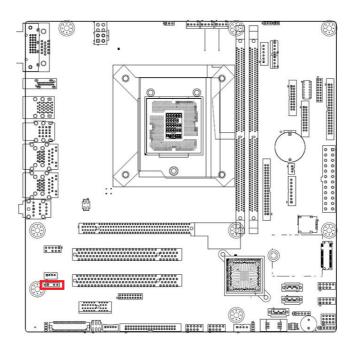
Note!



For motherboards with the optional HD Audio feature, we recommend that you connect a high-definition front panel audio module to this connector to take advantage of the motherboard's high definition audio capability.

2.18 Digital Audio Connector (SPDIF1)

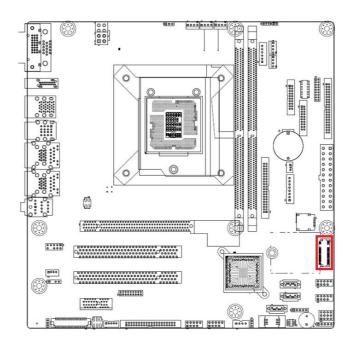
This connector is for the S/PDIF audio module to allow digital output sound. Connect one end of the S/PDIF audio cable to this connector and the other end to the S/PDIF module.



Note! The S/PDIF module should be purchased separately by end user



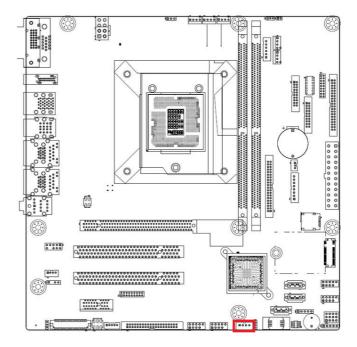
2.19 M.2 (B-Key/2242) (M2B1)



M.2 B-key: 2242, supports SATA or USB interface

2.20 SMBUS Header (SMBUS1)

AIMB-506 provides SMBUS connector for customer connection to SMBUS protocol embedded device. It can be configured to I2C by customer's request



Chapter

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings to control the special features of your computer. The Setup program uses a number of menus for making changes. This chapter describes the basic navigation of the AIMB-506 setup screens.

3.2 BIOS Setup

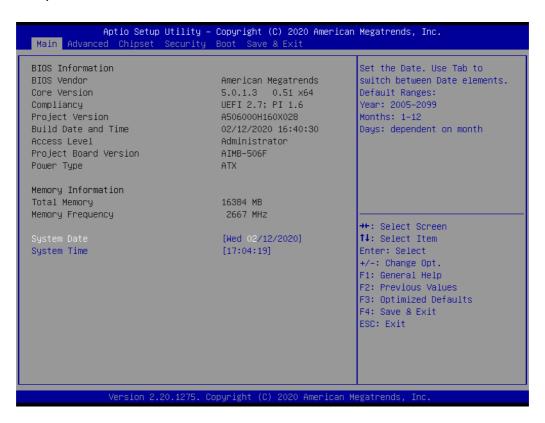
The AIMB-506 Series system has AMI BIOS built in, with a SETUP utility that allows users to configure required settings or to activate certain system features.

The SETUP saves the configuration in the FLASH of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the FLASH.

When the power is turned on, press the or <Esc> button during the BIOS POST (Power-On Self Test) to access the CMOS SETUP screen.

Control Keys	
< ← >< → >	Select Screen
< ↑ >< ↓ >	Select Item
<enter></enter>	Select
<+/->	Change Opt
<f1></f1>	General help
<f2></f2>	Previous Values
<f3></f3>	Optimized Defaults
<f4> <esc></esc></f4>	Save & Exit
<esc></esc>	Exit

Press or <Esc> to enter AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

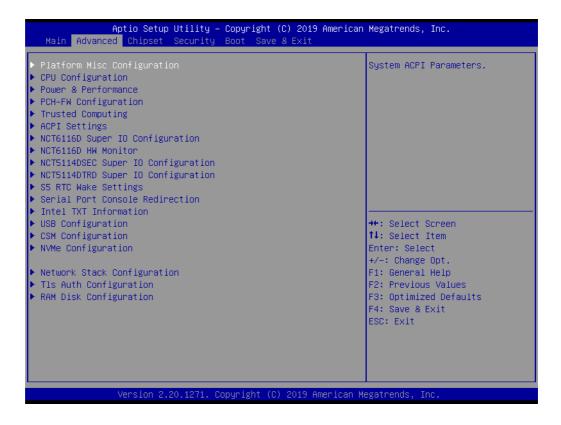
Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

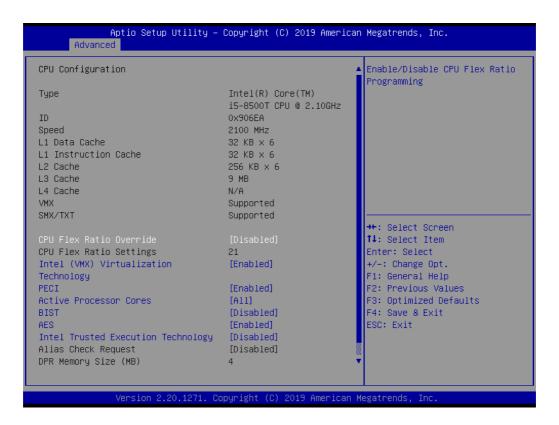
3.2.2 Advanced BIOS Features

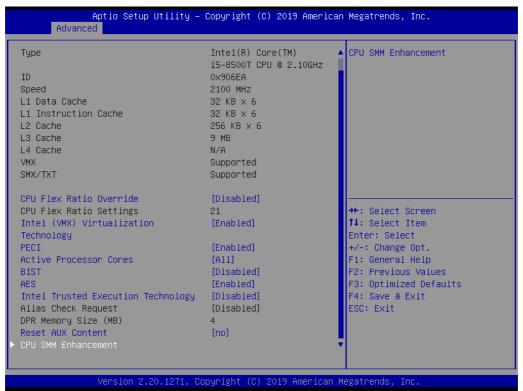
Select the Advanced tab from the AIMB-506 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

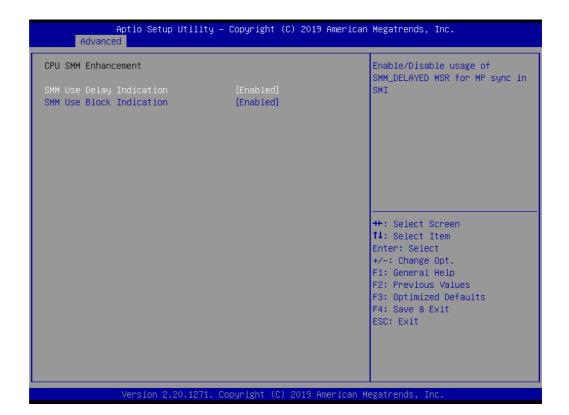


3.2.2.1 CPU Configuration

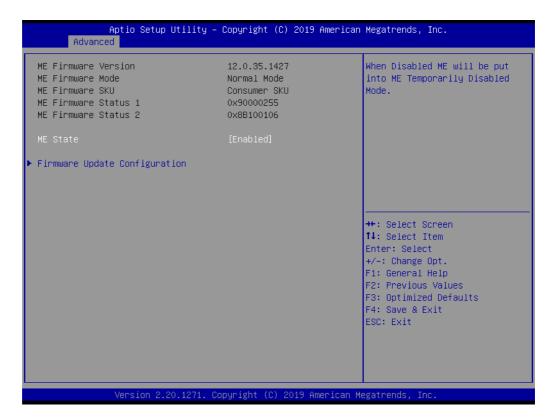
The item shows you CPU specification and feature, the content would be different for different CPU.







3.2.2.2 PCH FW Configuration



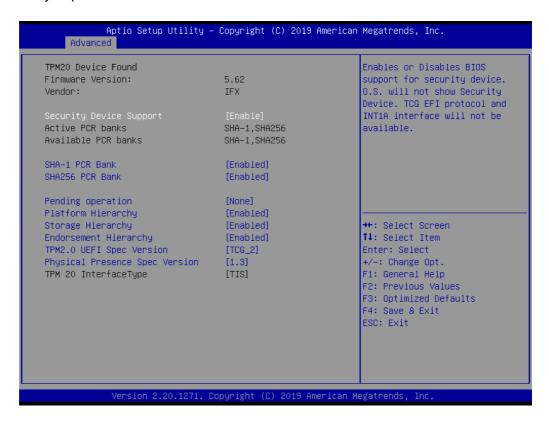
■ Firmware Update Configuration



- ME FW Image Re-Flash [Disabled]
- Local FW Update [Enabled]

3.2.2.3 Trusted Computing

To enable/disable TPM (TPM 1.2/2.0) set up in BIOS. TPM (Trusted Platform Module) is a secure key generator and key cache management component, enables protected storage of encryption keys and authentication credentials for enhanced security capabilities.

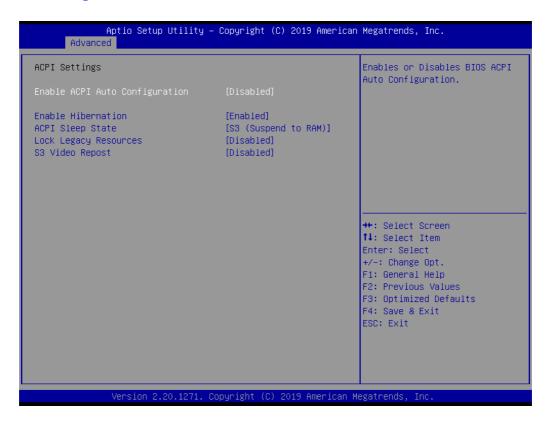


Security Device Support [Disable]

Note! TCG EFI Protocol and INT1A interface won't be available



3.2.2.4 ACPI Settings



■ Enable ACPI Auto Configuration [Disabled]

Enable or disable BIOS ACPI auto configuration

■ Enable Hibernation [Enabled

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State [Auto]

Select ACPI sleep state the system will enter when the SUSPEND button is pressed

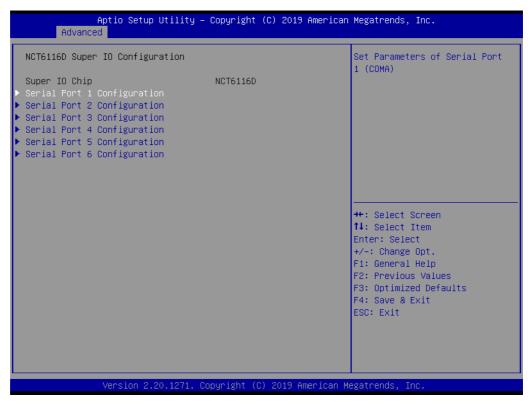
■ Lock Legacy Resources [Disabled]

Enables or Disables Lock of Legacy Resources

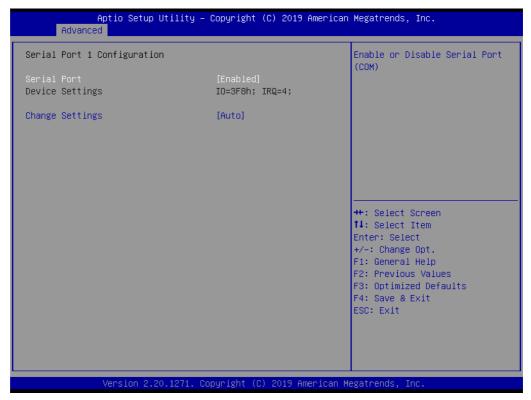
■ S3 Video Repost [Disabled]

Enable or Disable S3 Video Repost

3.2.2.5 NCT6116D Super I/O Configuration

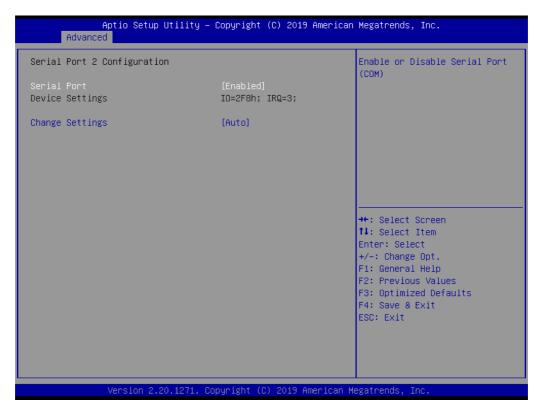


- Super I/O Chip [NCT6116D]
- Serial Port 1 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=3F8h; IRQ =4
- Change Settings [Auto]
 To select an optimal setting for serial port 1.

Serial Port 2 Configuration



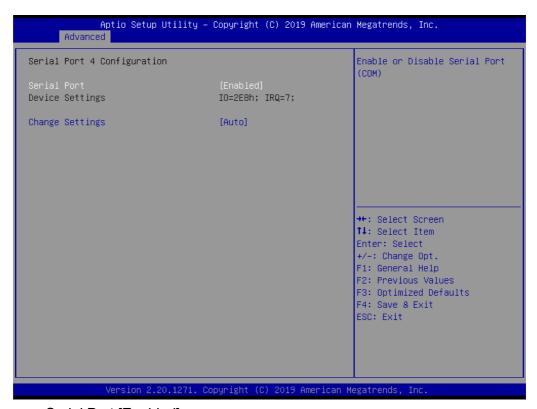
- Serial Port [Enabled]
- Device Settings: I/O=2F8h; IRQ =3
- Change Settings [Auto]
 To select an optimal setting for serial port 2.

Serial Port 3 Configuration



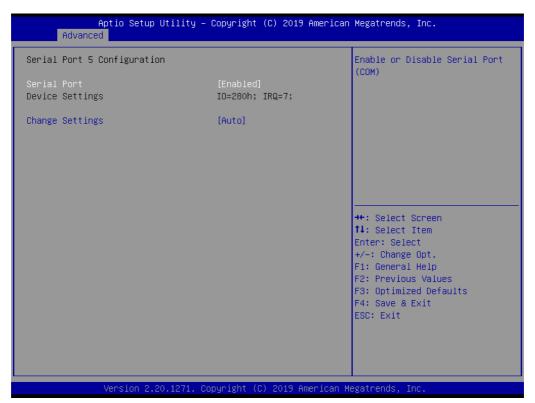
Serial Port [Enabled]

- Device Settings: I/O=3E8h; IRQ =7
- Change Settings [Auto]
- RS486 Auto Flow [Disabled]
 To select an optimal setting for serial port 3.
- Serial Port 4 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=2E8h; IRQ =7
- Change Settings [Auto]
 To select an optimal setting for serial port 4.

Serial Port 5 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=280h; IRQ =7
- Change Settings [Auto]
 To select an optimal setting for serial port 5.

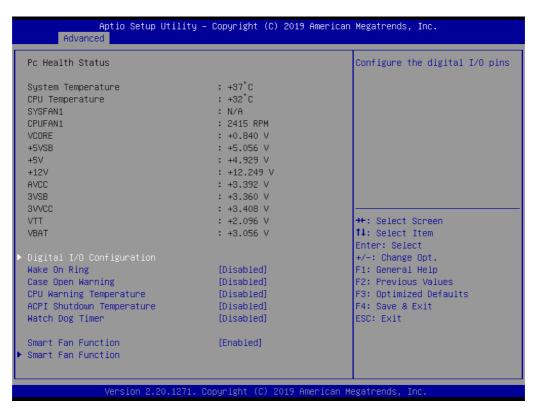
Serial Port 6 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=288h; IRQ =7
- Change Settings [Auto]
 To select an optimal setting for serial port 6.

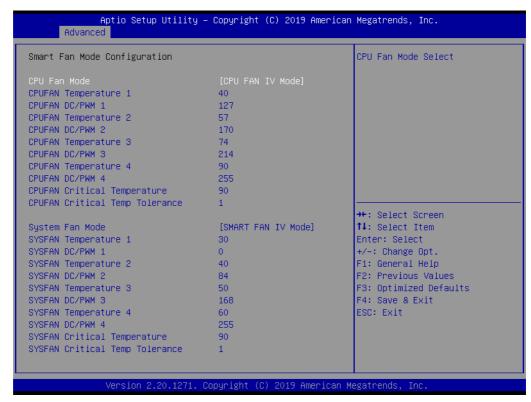
3.2.2.6 NCT6116D Configuration

■ PC Health Status



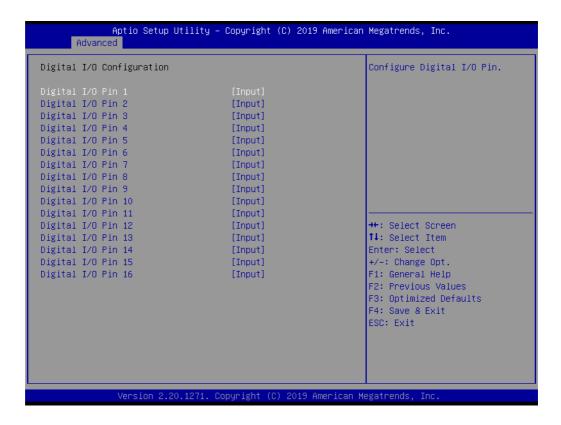
- CPU Warning Temperature [Disabled]
 Use this to set the CPU warning temperature threshold. When the system reaches the warning temperature, the speaker will beep.
- ACPI Shutdown Temperature [Disabled]
 Use this to set the ACPI shutdown temperature threshold. When the system reaches the shutdown temperature, it will be automatically shut down by ACPI OS to protect the system from overheating damage.

Smart Fan Mode Configuration



- CPU FAN Mode [SMART FAN IV Mode]
 The item shows you CPU temperature and fan speed (PWM) information.
- SYSFAN Mode [SMART FAN IV Mode]
 The item shows you system temperature and fan speed (PWM) information.

Digital I/O Configuration

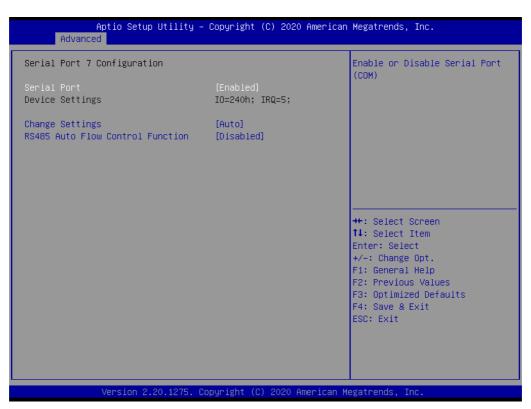


- Digital I/O Pin 1 - 16 [Input]

3.2.2.7 NCT5114DSEC Super I/O Configuration



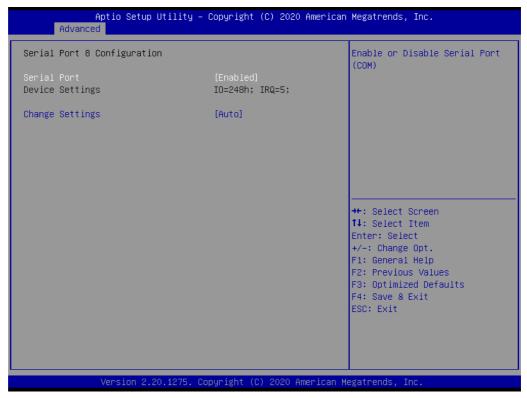
Serial Port 7 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=240h; IRQ =5
- Change Settings [Auto]

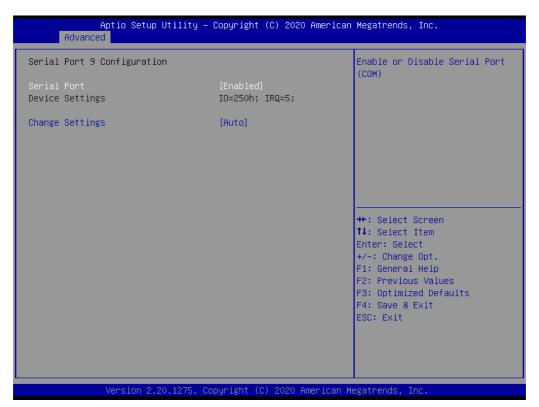
To select an optimal setting for serial port 7.

Serial Port 8 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=248h; IRQ =5
- Change Settings [Auto]
 To select an optimal setting for serial port 8.

Serial Port 9 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=250h; IRQ =5
- Change Settings [Auto]
 To select an optimal setting for serial port 9.

Serial Port 10 Configuration

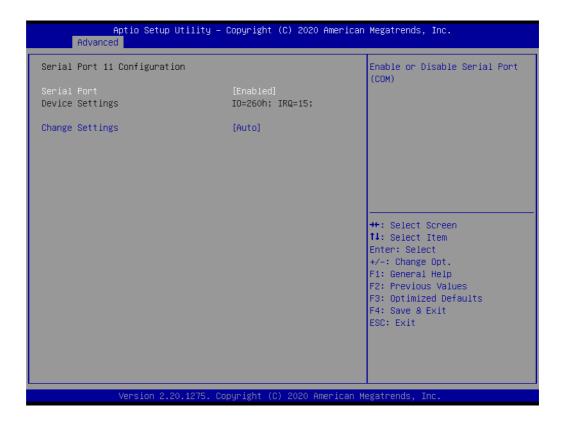


- Serial Port [Enabled]
- Device Settings: I/O=258h; IRQ =5
- Change Settings [Auto]
 To select an optimal setting for serial port 10.

3.2.2.8 NCT5114DTRD Super I/O Configuration

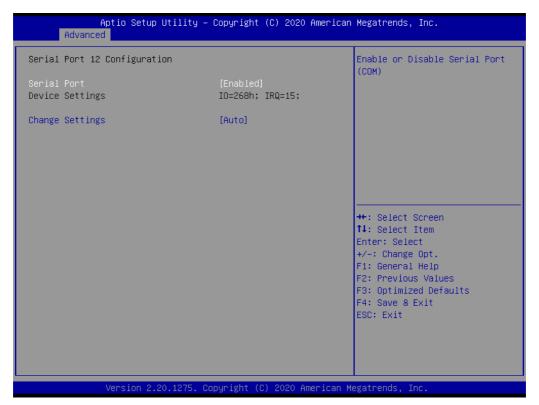


Serial Port 11 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=260h; IRQ =15
- Change Settings [Auto]
 To select an optimal setting for serial port 11.

Serial Port 12 Configuration



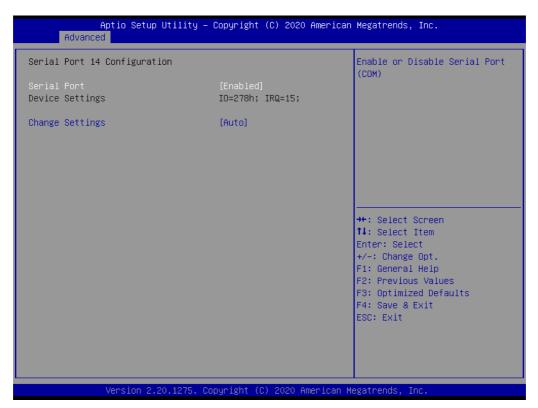
- Serial Port [Enabled]
- Device Settings: I/O=268h; IRQ =15
- Change Settings [Auto]
 To select an optimal setting for serial port 12.

Serial Port 13 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=270h; IRQ =15
- Change Settings [Auto]
 To select an optimal setting for serial port 13.

Serial Port 14 Configuration



- Serial Port [Enabled]
- Device Settings: I/O=278h; IRQ =15
- Change Settings [Auto] To select an optimal setting for serial port 14.

3.2.2.9 S5RTC Wake Settings

The item allows you enable or disable system wake up on alarm event.

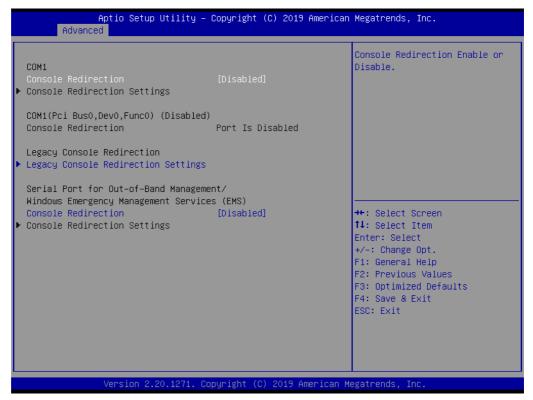


Wake system with Fixed Time [Disabled]

Note! When enabled, system will wake up on the specified time



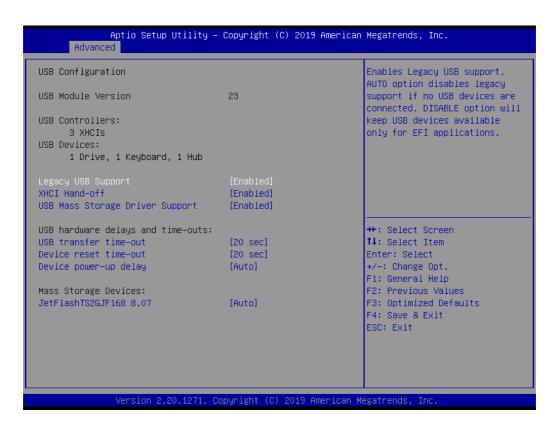
3.2.2.10 Serial Port Console Redirection



Console Redirection [Disabled]

Enable or disable the console redirection feature

3.2.2.11 USB Configuration

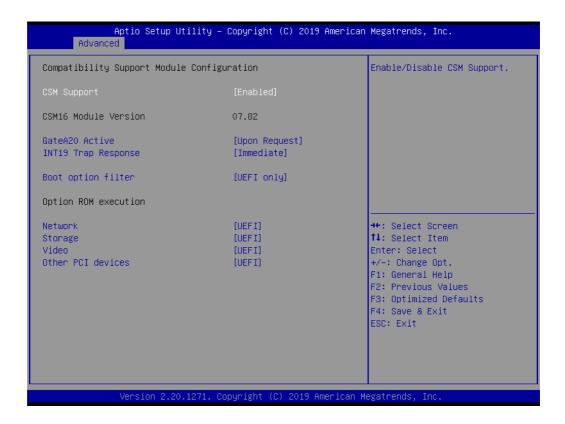


Legacy USB Support [Enabled]

Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.

- XHCI Hand-off [Enabled]
- **USB Mass Storage Driver Support [Enabled]**
- **USB** hardware delays and time-outs USB Device transfer & reset time-out and delay setting.
- **Mass Storage Devices [Auto]** Shows USB mass storage device information.

3.2.2.12 CSM Configuration



Boot option filter [UEFI only]
Network [UEFI]
Storage [UEFI]
Video [UEFI]
Other PCI device [UEFI]

Note!

If your HDD or other boot device is installed as Legacy mode, it may cause blue screen situation. There are 2 ways to solve this:



- 1. Re-install your OS as UEFI Mode
- 2. Change all of settings above as "Legacy"
- * Boot option filter-> Legacy Only
- * Network -> Legacy
- * Storage -> Legacy
- * Video -> Legacy
- * Other PCI devices -> Legacy

3.2.2.13 Network Stack Configuration [Disabled]



■ Enable/Disable UEFI Network Stack

Note! When network stack [enable], item must enable: LANx PXE OpROM [enable]

3.3 Chipset Configuration Settings

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item in the left frame of the screen, such as PCI express Configuration, to go to the sub menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub menus are described on the following pages.



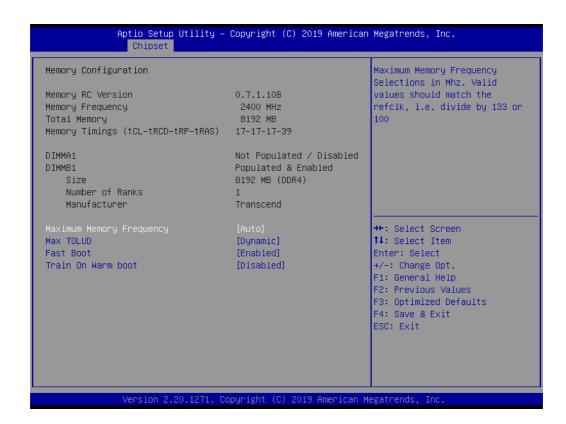
3.3.1 System Agent (SA) Configuration



■ VT-d [Enabled]

Disable or enable VT-d function on MCH.

3.3.1.1 Memory Configuration



The item shows you memory specification included RC version, Frequency, size and voltage information etc.

■ Max TOLUD [Dynamic]

Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

■ Retrain on Fast Fall [Enabled]

Enable or disable Retrain on Fast Fall.

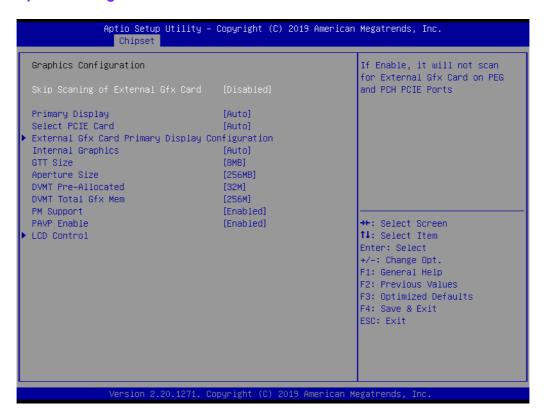
■ Memory Remap [Enabled]

Enable or disable Memory remap.

■ Fast Boot [Enabled]

Enable or disable Fast Boot support

3.3.1.2 Graphics Configuration



- Skip Scaning of External Gfx Card [Disabled]
- **Primary Display [Auto]**

Select which of IGFX/PEG/PCI Graphics device should be Primary Display

Internal Graphics [Auto]

Keep IGD enabled based on the setup options.

- GTT size [8MB]
- Aperture Size [256MB]
- **DVMT Pre-Allocated [32M]**

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

DVMT Total Gfx Mem [256M]

Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

Note! When BIOS set as " Auto", only a single display works under DOS.



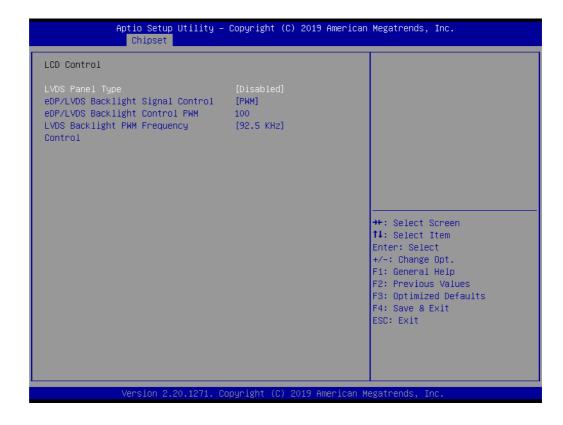
Note!

The dual display can only work under Windows 10, cannot work under DOS.



Below is the display combination table, all of these combinations are verified.

Display Combination List	BIOS	DOS	WES 8			
Single Display						
VGA	PASS	PASS	PASS			
DVI	PASS	PASS	PASS			
DP	PASS	PASS	PASS			
EDP/LVDS	PASS	PASS	PASS			
Dual Display						
VGA+DVI	NA	NA	PASS			
VGA+EDP/LVDS	NA	NA	PASS			
VGA+DP	NA	NA	PASS			
DVI+DP	NA	NA	PASS			
DVI+EDP/LVDS	NA	NA	PASS			
DP+EDP/LVDS	NA	NA	PASS			

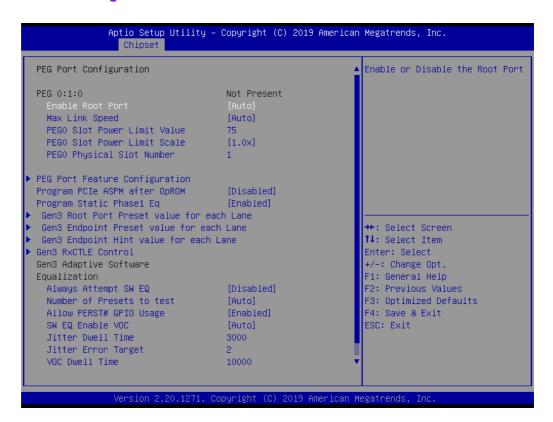


3.3.1.3 DMI Configuration



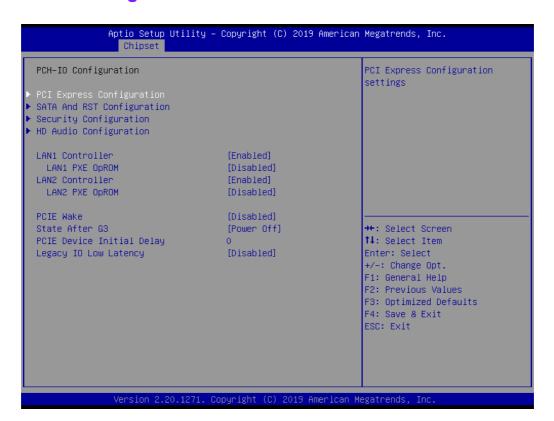
■ DMI MAx Link Speed [Auto]

3.3.1.4 PEG Port Configuration



- Enable Root Port [Auto]
- Max Link Speed [Auto]
- Detect Non-Compliance Device [Disabled]
 Detect Non-Compliance PCI Express Device in PEG
- Program PCle ASPM after OpROM [Disabled]
 Enabled: PCle ASPM will be programmed after OpROM.
 Disabled: PCle ASPM will be programmed before OpROM.
- Program Static Phase1 Eq [Enabled]
- PEG Gen3 Root Port Preset Value for each Lane
 Root Port Preset Value Per lane for Gen3 Equalization.
- PEG Gen3 Endpoint Preset Value for each Lane Endpoint Preset Value Per lane for Gen3 Equalization.
- PEG Gen3 Endpoint Hint Value each Lane
 Endpoint Hint Value Per lane for Gen3 Equalization.

3.3.2 PCH-IO Configuration



■ PCI Express Configuration

Details of PCI Express items. (See 3.3.2.1)

USB Configuration

Details of USB items. (See 3.3.2.2)

■ BIOS Security Configuration

Details of BIOS security items. (See 3.3.2.3)

LAN 1controller [Enabled]

Enable or disable the LAN 1 controller.

- LAN 2 controller [Enabled]
- PCIE Wake [Disabled]

Enable or disable PCIE to wake the system from S5.

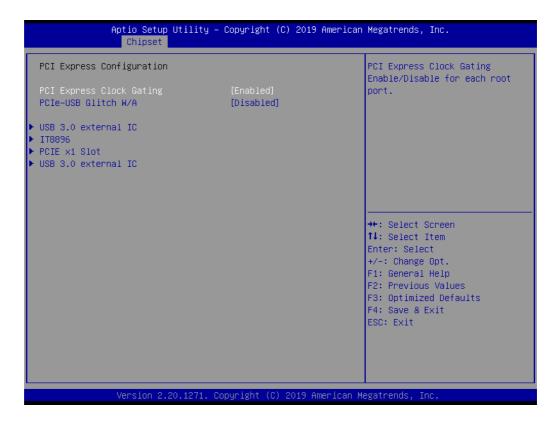
High Precision Timer

Enable or Disable High Precision Timer.

State After G3 [Power Off]

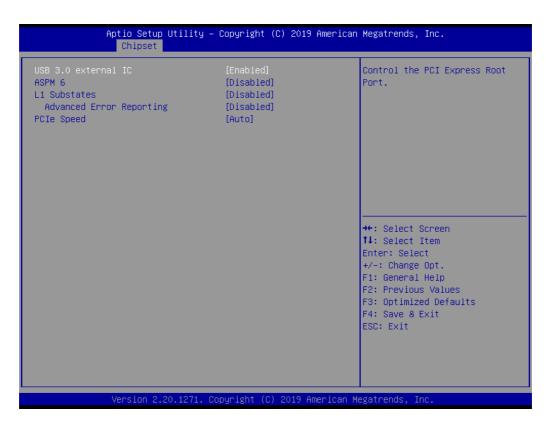
This item allows users to select off, on and last state.

3.3.2.1 PCI Express Configuration



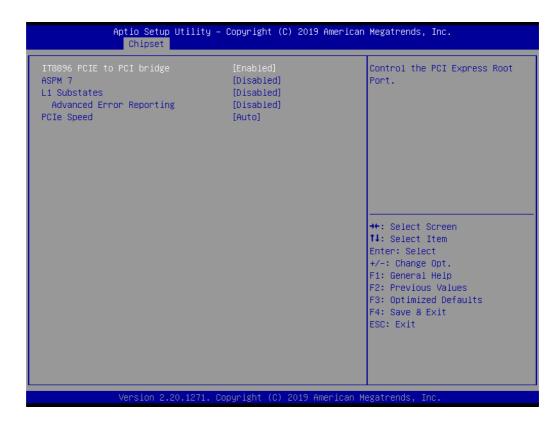
- PCI Express Clock Gating [Enabled]
 Enable or Disable PCI Express clock gating for each port.
- PCIe-USB Glitch W/A [Disabled]
 PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG Port.

■ USB 3.0 External IC



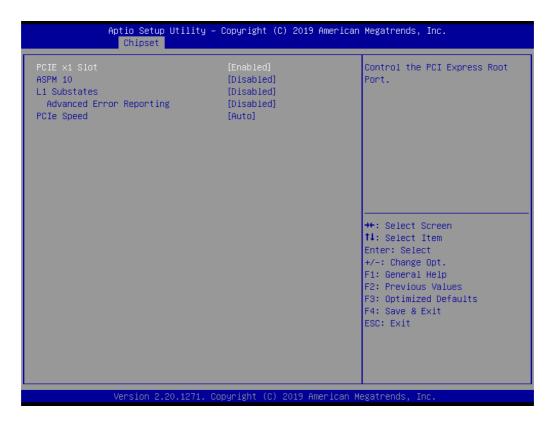
- USB3.0 External IC [Enabled]
 Control the PCI Express Root Port.
- ASPM Support [Auto]
 Set the ASPM Level: Force L0s Force all links to L0s State : AUTO BIOS auto configure : DISABLE Disables ASPM
- L1 Substates PCI Express L1 Substates settings.
- PCIe Speed [Auto]
 Select PCI Express port speed.

■ USB 3.0 External IC



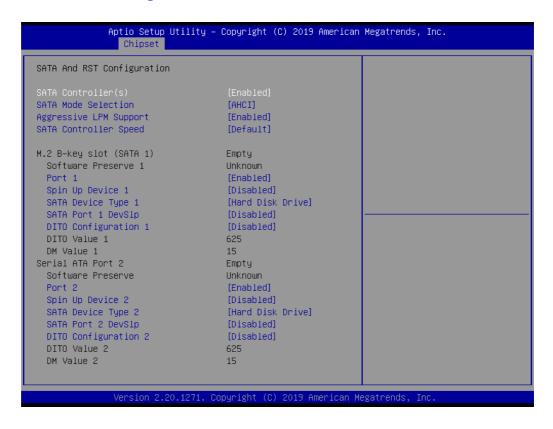
- ITE8896 PCIE to PCI Bridge [Enabled]
 Control the PCI Express Root Port.
- ASPM Support [Auto]
 Set the ASPM Level: Force L0s Force all links to L0s State : AUTO BIOS auto configure : DISABLE Disables ASPM
- L1 Substates PCI Express L1 Substates settings.
 PCIe Speed [Auto]
 Select PCI Express port speed.

■ PCI Express x1 Slot

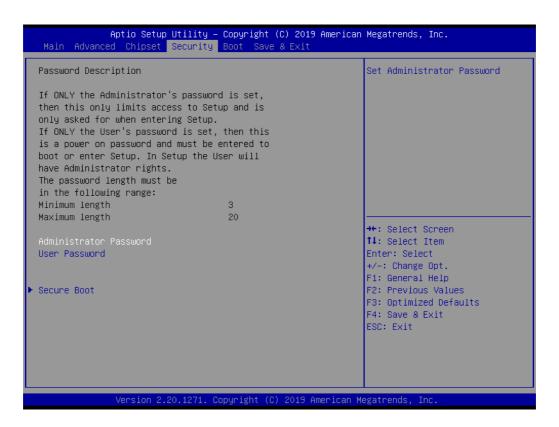


- PCI Express Root Port 1 [Enabled]
 Control the PCI Express Root Port.
- ASPM Support [Auto]
 Set the ASPM Level: Force L0s Force all links to L0s State : AUTO BIOS auto configure : DISABLE Disables ASPM
- L1 Substates PCI Express L1 Substates settings.
- PCle Speed [Auto]
 Select PCI Express port speed.

3.3.2.2 SATA and RST Configuration



3.4 Security Settings



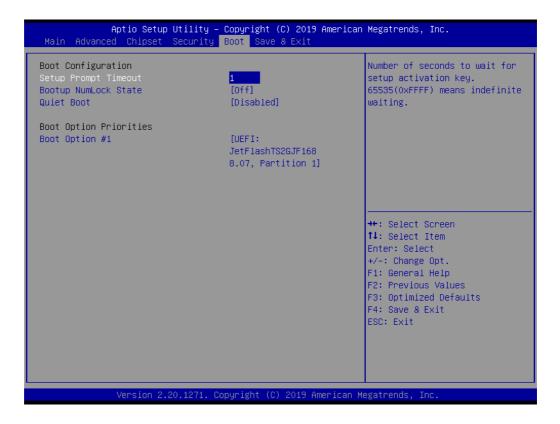
Administrator Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the Administrator password.

User Password

Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the User Password.

3.5 Boot Settings



Setup Prompt Timeout

User the <+> and <-> keys to adjust the number of seconds to wait for setup activation key.

Bootup NumLock State [On]

On or Off power on state for the NumLock

Quiet Boot [Disabled]

If this option is set to disabled, the BIOS displays normal POST messages. If enabled, an OEM logo is shown instead of POST messages.

■ Boot Option #1/#2

Choose boot priority from boot device

3.6 Save & Exit Configuration



Save Changes and Exit

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect of all system configuration parameters.

- Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
- 2. Select Ok or cancel.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

- Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
- 2. Select Ok to discard changes and exit. Discard Changes Select Discard Changes from the Exit menu and press <Enter>.

Save Changes and Reset

When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect of all system configuration parameters.

- Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
- 2. Select Ok or cancel.

Discard Changes and Reset

Select this option to quit Setup without making any permanent changes to the system configuration.

- 1. Select Reset Discarding Changes from the Exit menu and press <Enter>.
 The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
- 2. Select Ok to discard changes and reset. Discard Changes Select Discard Changes from the Exit menu and press <Enter>.

■ Restore Default

The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.

■ Save as User Default

Save the all current settings as a user default.

Restore User Default

Restore all settings to user default values.

Chapter

Software Introduction & Services

4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a set of user-friendly, intelligent and integrated interfaces, which speeds up development, enhances security, and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GPIO



SMBus



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

4.2.1.2 **Display**

Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 **Monitor**

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

4.2.1.4 Power Saving

CPU Speed



Makes use of Intel SpeedStep technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

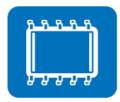
System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utility

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on the customers' disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

Monitoring



Monitoring is a utility for customers to monitor system health, like voltage, CPU and system temperature and fan speed. These items are important to a device, if critical errors occur and are not solved immediately, permanent damage may be caused.

Chapter

Chipset Software Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for AIMB-506 are located on Advantech website. (http://support.advantech.com/Support/.) Updates are provided via Service Packs from Microsoft*.

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel[®] Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- IDE Ultra ATA 100/66/33 and Serial ATA interface support
- Identification of Intel[®] chipset components in the Device Manager

Note!

This utility is used for the following versions of Windows, and it has to be installed **before** installing all the other drivers:



Windows 10 (64 bit)

5.3 Windows 10 Driver Setup

When enter the website of Advantech, then search product AIMB-506. There is "Chipset" driver inside.

Win10 driver for AIMB-506

Solution :

Released Date	Download Site
2020-02-18	Primary Secondary
2020-02-19	Primary Secondary
2020-02-19	Primary Secondary
2020-02-19	Primary Secondary
	2020-02-18 2020-02-18 2020-02-18 2020-02-18 2020-02-19 2020-02-19

Chapter

6

VGA Setup

6.1 Introduction

The Core i7/i5/i3, Pentium and Celeron CPUs are embedded with an integrated graphics controller. You need to install the VGA driver to enable this function.

Optimized integrated graphic solution: Intel Graphics, versatile display options and 32-bit 3D graphics engine are supported. Dual independent displays and enhanced display modes for widescreen flat panels include extended, twin, and clone dual display modes, plus optimized 3D support delivers an intensive and realistic visual experience.

6.2 Windows 10 VGA Driver Installation

Note!



Win10 driver for AIMB-506

Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.

Enter the Advantech website, then search product AIMB-506. There are "Graphic" drivers available.

Download File	Released Date	Download Site	
IMB-506_Chipset_Win10(64bit).zip	2020-02-18	Primary Seco	ondary
IMB-506_Graphics_Win10(64bit).zip	2020-02-18	Primary Seco	ondary
IMB-506_Realtek LAN_Win10(64bit).zip	2020-02-18	Primary Seco	ondary
NIMB-506_Intel ME AMT_Win10(64bit).zip	2020-02-18	Primary Seco	ondary
IMB-506_Audio_Win10(64bit).zip	2020-02-18	Primary Seco	ondary
IMB-506_Intel RAID AHCI_Win10(64bit).zip	2020-02-19	Primary Seco	ondary
IMB-506_Intel USB3.0_Win10(64bit).zip	2020-02-19	Primary Seco	ondary
MB-506_Intel Serial IO_Win10(64bit).zip	2020-02-19	Primary Seco	ondary

Chapter

LAN Configuration

7.1 Introduction

The AIMB-506 has dual Gigabit Ethernet LANs via dedicated PCI Express x1 lanes (Realtek 8111G) that offer bandwidth of up to 500 MB/sec, eliminating the bottleneck of network data flow and incorporating Gigabit Ethernet at 1000 Mbps.

7.2 Features

- Integrated 10/100/1000 Mbps transceiver
- 10/100/1000 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express X1 host interface

7.3 Installation

Note!



Before installing the LAN drivers, make sure the CSI utility has been installed on your system. See Chapter 5 for information on installing the CSI utility.

The AIMB-506's Realtek 8111G Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies from system to system. Please find and use the section that provides the driver setup procedure for the operating system you are using.

7.4 Windows® 10 Driver Setup (Realtek 8111G)

Enter the Advantech website, then search product AIMB-506. There is "LAN" driver inside.

Win10	driver	for	AIMB	-506
-------	--------	-----	------	------

Solution :

Download File	Released Date	Download Site
AIMB-506_Chipset_Win10(64bit).zip	2020-02-18	Primary Secondary
AIMB-506_Graphics_Win10(64bit).zip	2020-02-18	Primary Secondary
AIMB-506_Realtek LAN_Win10(64bit).zip	2020-02-18	Primary Secondary
AIMB-506_Intel ME AMT_Win10(64bit).zip	2020-02-18	Primary Secondary
AIMB-506_Audio_Win10(64bit).zip	2020-02-18	Primary Secondary
AIMB-506_Intel RAID AHCI_Win10(64bit).zip	2020-02-19	Primary Secondary
AIMB-506_Intel USB3.0_Win10(64bit).zip	2020-02-19	Primary Secondary
AIMB-506_Intel Serial IO_Win10(64bit).zip	2020-02-19	Primary Secondary

Appendix A

Programming the Watchdog Timer

A.1 Programming the Watchdog Timer

AIMB-506's watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and how to program it.

A.1.1 Watchdog Timer Overview

The watchdog timer is built into the super I/O controller Nuvoton NCT6116D. It provides the following user-programmable functions:

- Can be enabled and disabled by user program
- Timer can be set from 1 to 255 seconds or 1 to 255 minutes
- Generates an interrupt or resets signal if the software fails to reset the timer before time-out

A.1.2 Programming the Watchdog Timer

The I/O port address of the watchdog timer is 2E (hex) and 2F (hex). 2E (hex) is the address port. 2F (hex) is the data port. You must first assign the address of register by writing an address value into address port 2E (hex), then write/read data to/from the assigned register through data port 2F (hex).

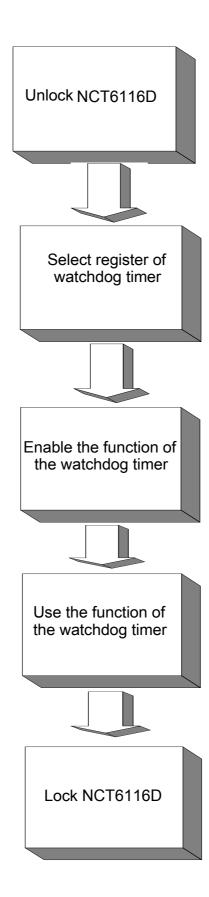


Table A.1: Watchdog Timer Registers

Ad	dress	of	Register	(2E)	Attribute
----	-------	----	----------	------	-----------

Read/Write	Value (2F) & description	
87 (hex)		Write this address to I/O address port 2E (hex) twice to unlock the NCT3779D.
07 (hex)	write	Write 08 (hex) to select register of watchdog timer.
30 (hex)	write	Write 01 (hex) to enable the function of the watchdog timer. Disabled is set as default.
F5 (hex)	write	Set seconds or minutes as units for the timer. Write 0 to bit 3: set second as counting unit. [default] Write 1 to bit 3: set minutes as counting unit.
F6 (hex)	write	0: stop timer [default] 01~FF (hex): The amount of the count, in seconds or minutes, depends on the value set in register F5 (hex). This number decides how long the watchdog timer waits for strobe before generating an interrupt or reset signal. Writing a new value to this register can reset the timer to count with the new value.
F7 (hex)	read/write	Bit 7:Write 1 to enable mouse to reset the timer, 0 to disable[default]. Bit 6: Write 1 to enable keyboard to reset the timer, 0 to disable.[default] Bit 5: Write 1 to generate a timeout signal immediately and automatically return to 0. [default=0] Bit 4: Read status of watchdog timer, 1 means timer is "timeout".
AA (hex)		Write this address to I/O port 2E (hex) to lock the watchdog timer 2.

A.1.3 Example Program

Enable watchdog timer and set 10 sec. as timeout interval Mov dx,2eh; Unlock NCT6779D Mov al,87h Out dx,al Out dx,al Mov al,07h; Select registers of watchdog timer Out dx,al Inc dx Mov al,08h Out dx,al Dec dx; Enable the function of watchdog timer Mov al,30h Out dx,al Inc dx Mov al,01h Out dx,al Dec dx; Set second as counting unit Mov al,0f5h Out dx,al Inc dx In al,dx And al, not 08h Out dx,al Dec dx; Set timeout interval as 10 seconds and start counting Mov al,0f6h Out dx,al Inc dx Mov al, 10 Out dx,al Dec dx; Lock NCT6779D Mov al,0aah Out dx,al Enable watchdog timer and set 5 minutes as timeout interval Mov dx,2eh; Unlock NCT6779D Mov al,87h Out dx,al Out dx,al

;	
Mov al,07h ; Select registers of watchdog timer Out dx,al Inc dx Mov al,08h Out dx,al ;	
Dec dx; Enable the function of watchdog timer Mov al,30h Out dx,al Inc dx Mov al,01h Out dx,al ;	
Dec dx; Set minute as counting unit Mov al,0f5h Out dx,al Inc dx In al,dx Or al,08h Out dx,al	
; Dec dx ; Set timeout interval as 5 minutes and start of Mov al,0f6h Out dx,al Inc dx Mov al,5 Out dx,al	counting
;Dec dx ; Lock NCT6779D Mov al,0aah Out dx,al 3. Enable watchdog timer to be reset by mouse	
; Mov dx,2eh ; Unlock NCT6779D Mov al,87h Out dx,al Out dx,al	
; Mov al,07h ; Select registers of watchdog timer Out dx,al Inc dx Mov al,08h Out dx,al ;	

Dec dx; Enable the function of watchdog timer Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al ;
Dec dx ; Enable watchdog timer to be reset by mouse
Mov al,0f7h
Out dx,al
Inc dx
In al,dx
Or al,80h
Out dx,al ;
Dec dx; Lock NCT6779D
Mov al,0aah
Out dx,al
4. Enable watchdog timer to be reset by keyboard ;
Mov dx,2eh ; Unlock NCT6779D
Mov al,87h
Out dx,al
Out dx,al ;
Mov al,07h; Select registers of watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al ;
Dec dx ; Enable the function of watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al ;
Dec dx ; Enable watchdog timer to be strobed reset by keyboard
Mov al,0f7h
Out dx,al
Inc dx
In al,dx
Or al,40h
Out dx,al

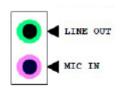
Dec dx ; Lock NCT6779D
Mov al,0aah
Out dx,al
5. Generate a time-out signal without timer counting
Mov dx,2eh ; Unlock NCT6779D
Mov al,87h
Out dx,al
Out dx,al
;
Mov al,07h; Select registers of watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
;
Dec dx; Enable the function of watchdog timer Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;
Dec dx ; Generate a time-out signal
Mov al,0f7h
Out dx,al ;Write 1 to bit 5 of F7 register
Inc dx
In al,dx
Or al,20h
Out dx,al
;Dec dx ; Lock NCT6779D
Mov al,0aah

Out dx,al

Appendix B

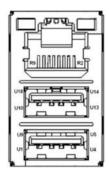
Pin Assignments

B.1 HD Audio Interface (AUDIO1)



Pin	Signal
1	MIC IN
2	LINE OUT

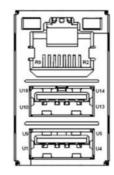
B.2 LAN & USB3.0 Connector (LAN2_USB34)



Pin	Signal	Pin	Signal
R1	LAN2_VCT	R8	LAN2_MDI3+
R2	LAN2_MDI0+	R9	LAN2_MDI3-
R3	LAN2_MDI0-	R10	GND
R4	LAN2_MDI1+	L1	LAN2_ACT
R5	LAN2_MDI1-	L2	+V3.3_LAN2
R6	LAN2_MDI2+	L3	LAN2_LED1_1G#
R7	LAN2_MDI2-	L4	LAN2_LED2_100M#

Pin	Signal	Pin	Signal
U1	+USBV2	U10	+USBV2
U2	D3-	U11	D4-
U3	D3+	U12	D4+
U4	GND	U13	GND
U5	RX-3	U14	RX-4
U6	RX+3	U15	RX+4
U7	GND	U16	GND
U8	TX-3	U17	TX-4
U9	TX+3	U18	TX+4

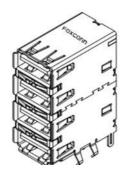
B.3 LAN & USB3.0 Connector (LAN1_USB12)



Pin	Signal	Pin	Signal
R1	LAN1_VCT	R8	LAN1_MDI3+
R2	LAN1_MDI0+	R9	LAN1_MDI3-
R3	LAN1_MDI0-	R10	GND
R4	LAN1_MDI1+	L1	LAN1_ACT
R5	LAN1_MDI1-	L2	+V3.3_LAN1
R6	LAN1_MDI2+	L3	LAN1_LED1_1G#
R7	LAN1_MDI2-	L4	LAN1_LED2_100M#

Pin	Signal	Pin	Signal	
U1	+USBV1	U10	+USBV1	
U2	D1-	U11	D2-	
U3	D1+	U12	D2+	
U4	GND	U13	GND	
U5	RX-1	U14	RX-2	
U6	RX+1	U15	RX+2	
U7	GND	U16	GND	
U8	TX-1	U17	TX-2	
U9	TX+1	U18	TX+2	

B.4 USB2.0 Connector (USB5678)



Pin	Signal	Pin	Signal
A1	+USBV3	C1	+USBV4
A2	USB_CM_N5	C2	USB_CM_N7
A3	USB_CM_P5	C3	USB_CM_P7
A4	GND	C4	GND
B1	+USBV3	D1	+USBV4
B2	USB_CM_N6	D2	USB_CM_N8
B3	USB_CM_P6	D3	USB_CM_P8
B4	GND	D4	GND

B.5 USB3.0 Connector (USB9101112)

Pin	Signal	Pin	Signal
11	+USBV5	31	+USBV6
12	USBPCIE_z_P1-	32	USBPCIE_z_P3-
13	USBPCIE_z_P1+	33	USBPCIE_z_P3+
14	GND	34	GND
15	USB3D1_z_RX-	35	USB3D3_z_RX-
16	USB3D1_z_RX+	36	USB3D3_z_RX+
17	GND	37	GND
18	USB3D1_z_TX-	38	USB3D3_z_TX-
19	USB3D1_z_TX+	39	USB3D3_z_TX+
21	+USBV5	41	+USBV6
22	USBPCIE_z_P2-	42	USBPCIE_z_P4-
23	USBPCIE_z_P2+	43	USBPCIE_z_P4+
24	GND	44	GND
25	USB3D2_z_RX-	45	USB3D4_z_RX-
26	USB3D2_z_RX+	46	USB3D4_z_RX+
27	GND	47	GND
28	USB3D2_z_TX-	48	USB3D4_z_TX-
29	USB3D2_z_TX+	49	USB3D4_z_TX+

B.6 Display Port Connector (DP1)



Pin	Signal	Pin	Signal
1	DP1_0+	11	GND
2	GND	12	DP1_3-
3	DP1_0-	13	DP1_AUX_EN#
4	DP1_1+	14	GND
5	GND	15	DP1_AUX+
6	DP1_1-	16	GND
7	DP1_2+	17	DP1_AUX-
8	GND	18	DP1_HPD
9	DP1_2-	19	GND
10	DP1_3+	20	+V3.3_DP1

B.7 VGA & DVI Connector (VGA1+DVI1)



Pin	Signal	Pin	Signal
1	DVI1_D0-	13	GND
2	DVI1_D0+	14	+VCC_TMDS
3	GND	15	GND
4	GND	16	DVI1_HPD
5	GND	17	DVI1_D2-
6	DVI1_SCL	18	DVI1_D2+
7	DVI1_SDA	19	GND
8	GND	20	GND
9	DVI1_D1-	21	GND
10	DVI1_D1+	22	GND
11	GND	23	DVI1_D3+
12	GND	24	DVI1_D3-

Pin	Signal	Pin	Signal
D1	VGA1_b_R	D9	+VCC_TMDS
D2	VGA1_b_G	D10	GND
D3	VGA1_b_B	D11	NC
D4	CLKREQ#	D12	VGA1_a_DDAT
D5	GND	D13	VGA1_b_HS
D6	VGA1_FOC_ON	D14	VGA1_b_VS
D7	GND	D15	VGA1_a_DCLK
D8	GND		

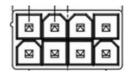
B.8 ATX 4/8 Pin Main Power Connector (ATX12V1 / ATX12V2)

ATX12V1



Pin	Signal	Pin	Signal
1	GND	3	+12V
2	GND	4	+12V

ATX12V2

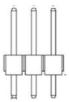


Pin	Signal	Pin	Signal	
1	GND	5	+12V	
2	GND	6	+12V	
3	GND	7	+12V	
4	GND	8	+12V	

B.9 CPU Socket LGA 1151 H4 (CPU1)

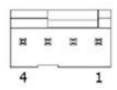


B.10 SMBUS Header (JSMB2)



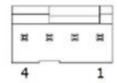
Pin	Signal	Pin	Signal
1	CPU_SDA	3	CPU_SCL
2	GND		

B.11 CPU FAN Header (CPUFAN1)



Pin	Signal	Pin	Signal
1	GND	3	CPU FAN SPEED
2	CPU FAN VCC	4	CPU FAN PWM

B.12 SYSTEM FAN Header (SYSFAN1)



Pin	Signal	Pin	Signal
1	GND	3	SYSTEM FAN SPEED
2	SYSTEM FAN VCC	4	SYSTEM FAN PWM

B.13 SYSTEM FAN Header (SYSFAN2)



Pin	Signal	Pin	Signal
1	GND	3	SYSTEM FAN_SPEED
2	SYSTEM FAN VCC	4	SYSTEM FAN PWM

B.14 DDR4 DIMM Socket (DIMMA1)

Please see JEDEC STANDARD.

B.15 DDR4 DIMM Socket (DIMMB1)

Please see JEDEC STANDARD.

B.16 Case Open Switch Pin Header (JCASEOP_SW1)



Pin	Signal	Pin	Signal
1	Normal Open	3	Normal Close
2	Advantech define		

B.17 Case Open Pin Header (JCASE1)



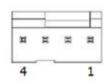
Pin	Signal	Pin	Signal
1	Case Open	2	GND

B.18 Keyboard Mouse Pin Header (KBMS1)



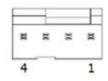
Pin	Signal	Pin	Signal
1	KB_CLK#	4	GND
2	KB_DAT#	5	+V5_DUAL
3	MS_CLK#	6	MS_DAT#

B.19 SYSTEM FAN Header (SYSFAN3)



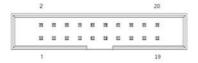
Pin	Signal	Pin	Signal
1	GND	3	SYSTEM FAN SPEED
2	SYSTEM FAN VCC	4	SYSTEM FAN PWM

B.20 SYSTEM FAN Header (SYSFAN4)



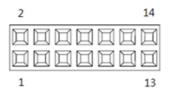
Pin	Signal	Pin	Signal
1	GND	3	SYSTEM FAN SPEED
2	SYSTEM FAN VCC	4	SYSTEM FAN PWM

B.21 COM Port Pin Header (COM12)



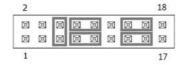
Pin	Signal	Pin	Signal
1	COM1_DCD#	11	COM2_DCD#
2	COM1_DSR#	12	COM2_DSR#
3	COM1_SIN	13	COM2_SIN
4	COM1_RTS#	14	COM2_RTS#
5	COM1_SOUT	15	COM2_SOUT
6	COM1_CTS#	16	COM2_CTS#
7	COM1_DTR#	17	COM2_DTR#
8	COM1_RI_V#	18	COM2_RI_V#
9	GND	19	GND
10	GND	20	GND

B.22 LPC Pin Header (LPC1)



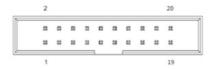
Pin	Signal	Pin	Signal
1	CLK (24MHz)	8	GND
2	AD1	9	AD2
3	RESET#	10	SMB CLK
4	AD0	11	SERIRQ
5	FRAME#	12	SMB DAT
6	+3.3V	13	+V5_DUAL
7	AD3	14	+5V

B.23 COM3456 Setting Pin Header (JSETCOM3)



Pin	Signal	Pin	Signal
1	UART_SIN	10	COM_SOUT
2	RXDRS485	11	COM_TXD485-
3	UART_SIN	12	COM_RXD485+
4	RXDRS422	13	SIN
5	UART_SIN	14	DTR
6	RXDRS232	15	COM_SIN
7	DCD	16	COM_DTR#
8	SOUT	17	COM_TXD485+
9	DCD#	18	COM_RXD485-

B.24 General Purpose I/O Pin Header (GPIO1)



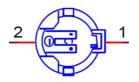
Pin	Signal	Pin	Signal
1	GPIO0	11	GPIO5
2	GPIO8	12	GPIO13
3	GPIO1	13	GPIO6
4	GPIO9	14	GPIO14
5	GPIO2	15	GPIO7
6	GPIO10	16	GPIO15
7	GPIO3	17	+V5_DUAL
8	GPIO11	18	GND
9	GPIO4	19	+V5_DUAL
10	GPIO12	20	GND

B.25 COM Port Pin Header (COM3456)



Signal	Pin	Signal
DCD# [3]	2	DSR# [3]
RXD [3]	4	RST# [3]
TXD [3]	6	CTS# [3]
DTR# [3]	8	RI# [3]
GND	10	GND
DCD# [4]	12	DSR# [4]
RXD [4]	14	RST# [4]
TXD [4]	16	CTS# [4]
DTR# [4]	18	RI# [4]
GND	20	GND
DCD# [5]	22	DSR# [5]
RXD [5]	24	RST# [5]
TXD [5]	26	CTS# [5]
DTR# [5]	28	RI# [5]
GND	30	GND
DCD# [6]	32	DSR# [6]
RXD [6]	34	RST# [6]
TXD [6]	36	CTS# [6]
DTR# [6]	38	RI# [6]
GND	40	GND
	DCD# [3] RXD [3] TXD [3] DTR# [3] GND DCD# [4] RXD [4] TXD [4] DTR# [4] GND DCD# [5] RXD [5] TXD [5] DTR# [5] GND DCD# [6] RXD [6] TXD [6] DTR# [6]	DCD# [3] 2 RXD [3] 4 TXD [3] 6 DTR# [3] 8 GND 10 DCD# [4] 12 RXD [4] 14 TXD [4] 16 DTR# [4] 18 GND 20 DCD# [5] 22 RXD [5] 24 TXD [5] 26 DTR# [5] 28 GND 30 DCD# [6] 32 RXD [6] 34 TXD [6] 36 DTR# [6] 38

B.26 Battery Holder (BAT1)



Pin	Signal	Pin	Signal
1	VBAT	2	GND

B.27 AT/ATX Mode Selection Header (PSON1)



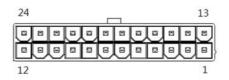
Pin	Signal	Pin	Signal
1	AT	3	ATX
2	+3.3V		

B.28 Alarm Board/CMM Power Pin Header (VOLT1)



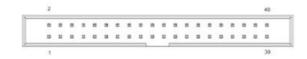
Pin	Signal	Pin	Signal
1	+5VSB	5	+5V
2	GND	6	+3.3V
3	GND	7	-12V
4	-5V	8	+12V

B.29 ATX Power Header (EATXPWR1)



Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PSON#
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWROK	20	-5V
9	+5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

B.30 COM Port Pin Header (COM11121314)



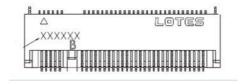
Pin	Signal	Pin	Signal
1	DCD# [11]	2	DSR# [11]
3	RXD [11]	4	RST# [11]
5	TXD [11]	6	CTS# [11]
7	DTR# [11]	8	RI# [11]
9	GND	10	GND
11	DCD# [12]	12	DSR# [12]
13	RXD [12]	14	RST# [12]
15	TXD [12]	16	CTS# [12]
17	DTR# [12]	18	RI# [12]
19	GND	20	GND
21	DCD# [13]	22	DSR# [13]
23	RXD [13]	24	RST# [13]
25	TXD [13]	26	CTS# [13]
27	DTR# [13]	28	RI# [13]
29	GND	30	GND
31	DCD# [14]	32	DSR# [14]
33	RXD [14]	34	RST# [14]
35	TXD [14]	36	CTS# [14]
37	DTR# [14]	38	RI# [14]
39	GND	40	GND

B.31 SIM Card Holder (SIM1)



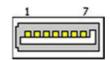
Pin	Signal	Pin	Signal
1	UIM_PWR	4	GND
2	UIM_RESET	5	UIM_VPP
3	UIM_CLK	6	UIM_DATA

B.32 M.2 B Key Socket (M2B1)



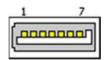
Pin	Signal	Pin	Signal	
1	CONFIG_3	2	+3.3V	
3	GND	4	+3.3V	
5	GND	6	FULL_CARD_POWER_OFF#	
7	USB_D+	8	W_DISABLE1#	
9	USB_D-	10	LED	
11	GND	12	Connector KEY	
13	Connector KEY	14	Connector KEY	
15	Connector KEY	16	Connector KEY	
17	Connector KEY	18	Connector KEY	
19	Connector KEY	20	NC	
21	CONFIG_0	22	NC	
23	PCIE_WAKE#	24	NC	
25	DPR	26	M.2_GNSS_DISABLE#	
27	GND	28	NC	
29	NC	30	UIM-RESET (I)	
31	NC	32	UIM-CLK (I)	
33	GND	34	UIM-DATA (I/O)	
35	NC	36	UIM-PWR (I)	
37	NC	38	SATA_DEVSLP (O)	
39	GND	40	M.2_ISH_SCL	
41	SATA_B+	42	M.2_ISH_SDA	
43	SATA_B-	44	NC	
45	GND	46	NC	
47	SATA_A-	48	NC	
49	SATA_A+	50	NC	
51	GND	52	NC	
53	NC	54	NC	
55	NC	56	NC	
57	GND	58	NC	
59	NC	60	NC	
61	NC	62	NC	
63	NC	64	NC	
65	NC	66	NC	
67	RESET#	68	SUSCLK(32kHz)	
69	CONFIG_1	70	+3.3V	
71	GND	72	+3.3V	
73	GND	74	+3.3V	
75	CONFIG_2			

B.33 SATA Connector (SATA1)



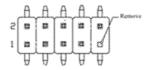
Pin	Signal	Pin	Signal	
1	GND	5	RX-	
2	TX+	6	RX+	
3	TX-	7	GND	
4	GND			

B.34 SATA Connector (SATA2)



Pin	Signal	Pin	Signal
1	GND	5	RX-
2	TX+	6	RX+
3	TX-	7	GND
4	GND		

B.35 USB2.0 Pin Header (USB1920)



Pin	Signal	Pin	Signal
1	VBUS	2	VBUS
3	USBPCIE_z_P3_b-	4	USBPCIE_z_P4_b-
5	USBPCIE_z_P3_b+	6	USBPCIE_z_P4_b+
7	GND	8	GND
9	NC	10	NC

B.36 USB2.0 Pin Header (USB1718)



Pin	Signal	Pin	Signal
1	VBUS	2	VBUS
3	USBPCIE_z_P1_b-	4	USBPCIE_z_P2_b-
5	USBPCIE_z_P1_b+	6	USBPCIE_z_P2_b+
7	GND	8	GND
9	NC	10	NC

B.37 Front Panel Header (JFP1)



Pin	Signal	Pin	Signal
1	+5V	2	HDD LED+
3	Power Button+	4	SPK_P2
5	HDD LED-	6	Power Button-
7	SPK_P3	8	SMB_DATA
9	System Reset+	10	SPK_P4
11	SMB_CLK	12	System Reset-

B.38 Watchdog & Beep Pin Header (JWDT1+JOBS1)



Pin	Signal
1	NC
2	Watch Dog Reset# output
3	System Reset input#
4	SIO Warning Beep output
5	SP1 Buzzer Beep input

B.39 Speaker (SP1)

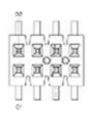


B.40 PLED Pin Header (JFP2)



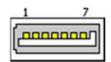
Pin	Signal
1	LED Power
2	NC
3	SIO_SUSLED
4	Keyboard Lock
5	GND

B.41 SPI Programming Pin Header (SPI_CN1)



Pin	Signal	Pin	Signal
1	+V3.3_SPI	2	GND
3	CS#	4	SCLK
5	MISO	6	MOSI
7	GND	8	NC

B.42 SATA Connector (SATA3)



Pin	Signal	Pin	Signal
1	GND	5	RX-
2	TX+	6	RX+
3	TX-	7	GND
4	GND		

B.43 SPI ROM Socket (SPI1)



Pin	Signal	Pin	Signal
1	CS#	5	MOSI
2	MISO	6	SCLK
3	WP# / IO2	7	HOLD# / IO3
4	GND	8	+V3.3_SPI

B.44 Clear CMOS Pin Header (JCMOS1)



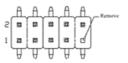
Pin	Signal
1	VBAT
2	RTC RESET#
3	GND

B.45 SMbus Pin Header (SMBUS1)



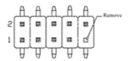
Pin	Signal
1	+5VSB
2	SMB CLK
3	SMB DAT
4	GND

B.46 USB2.0 Pin Header (USB1516)



Pin	Signal	Pin	Signal
1	VBUS	2	VBUS
3	USB_HCM_N3	4	USB_HCM_N4
5	USB_HCM_P3	6	USB_HCM_P4
7	GND	8	GND
9	NC	10	NC

B.47 USB2.0 Pin Header (USB1314)



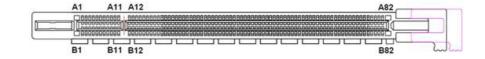
Pin	Signal	Pin	Signal
1	VBUS	2	VBUS
3	USB_HCM_N1	4	USB_HCM_N2
5	USB_HCM_P1	6	USB_HCM_P2
7	GND	8	GND
9	NC	10	NC

B.48 COM Port Pin Header (COM78910)



Pin	Signal	Pin	Signal
1	DCD# [7]	2	DSR# [7]
3	RXD [7]	4	RST# [7]
5	TXD [7]	6	CTS# [7]
7	DTR# [7]	8	RI# [7]
9	GND	10	GND
11	DCD# [8]	12	DSR# [8]
13	RXD [8]	14	RST# [8]
15	TXD [8]	16	CTS# [8]
17	DTR# [8]	18	RI# [8]
19	GND	20	GND
21	DCD# [9]	22	DSR# [9]
23	RXD [9]	24	RST# [9]
25	TXD [9]	26	CTS# [9]
27	DTR# [9]	28	RI# [9]
29	GND	30	GND
31	DCD# [10]	32	DSR# [11]
33	RXD [10]	34	RST# [10]
35	TXD [10]	36	CTS# [10]
37	DTR# [10]	38	RI# [10]
39	GND	40	GND

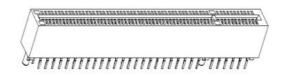
B.49 PCIe x16 Slot (PCIEX16_1)



B1 +12V A1 PRSNT1# B2 +12V A2 +12V B3 +12V A3 +12V B4 GND A4 GND B5 SMB_CLK A5 Reserved B6 SMB_DATA A6 Reserved	
B3 +12V A3 +12V B4 GND A4 GND B5 SMB_CLK A5 Reserved	
B4 GND A4 GND B5 SMB_CLK A5 Reserved	
B5 SMB_CLK A5 Reserved	
_	
B6 SMB DATA A6 Reserved	
Citiz_D/(i/t //o //coerved	
B7 GND A7 Reserved	
B8 +3.3V A8 Reserved	
B9 Reserved A9 +3.3V	
B10 +3.3VAUX A10 +3.3V	
B11 WAKE# A11 PWRGD	
B12 Reserved A12 GND	
B13 GND A13 REFCLK+	
B14 TX0+ A14 REFCLK-	
B15 TX0- A15 GND	
B16 GND A16 RX0+	
B17 Advantech define A17 RX0-	
B18 Advantech define A18 GND	
B19 TX1+ A19 Reserved	
B20 TX1- A20 GND	
B21 GND A21 RX1+	
B22 GND A22 RX1-	
B23 TX2+ A23 GND	
B24 TX2- A24 GND	
B25 GND A25 RX2+	
B26 GND A26 RX2-	
B27 TX3+ A27 GND	
B28 TX3- A28 GND	
B29 GND A29 RX3+	
B30 Reserved A30 RX3-	
B31 Reserved A31 GND	
B32 GND A32 Reserved	
B33 TX4+ A33 Reserved	
B34 TX4- A34 GND	
B35 GND A35 RX4+	
B36 GND A36 RX4-	
B37 TX5+ A37 GND	
B38 TX5- A38 GND	
B39 GND A39 RX5+	
B40 GND A40 RX5-	

B41	TX6+	A41	GND
B42	TX6-	A42	GND
B43	GND	A43	RX6+
B44	GND	A44	RX6-
B45	TX7+	A45	GND
B46	TX7-	A46	GND
B47	GND	A47	RX7+
B48	Reserved	A48	RX7-
B49	GND	A49	GND

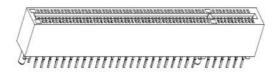
B.50 PCI Slot (PCI1)



Pin	Signal	Pin	Signal
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	NC	A4	TDI
B5	+5V	A5	+V5
B6	+5V	A6	INT#A
B7	INT#B	A7	INT#C
B8	INT#D	A8	+V5
B9	CLK33M_PCI2	A9	GNT#1
B10	PCI_REQ#1	A10	+V5
B11	CLK33M_PCI3	A11	GNT#2
B12	GND	A12	GND
B13	GND	A13	GND
B14	PCI_REQ#2	A14	+V3.3_DUAL
B15	GND	A15	RST#
B16	CLK33M_PCI1	A16	+V5
B17	GND	A17	GNT#0
B18	PCI_REQ#0	A18	GND
B19	+V5	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	+V3.3
B22	GND	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND
B25	+V3.3	A25	AD24
B26	PCI_CBE#3	A26	AD16
B27	AD23	A27	+V3.3
B28	GND	A28	AD22

B29 AD21 A29 B30 AD19 A30 B31 +V3.3 A31 B32 AD17 A32 B33 PCI CBE#2 A33	AD20 GND AD18 AD16 +V3.3
B32 AD17 A32	AD16
B33 DCI CBE#3 A33	+V3.3
DOS FOI_CDE#2 ASS	
B34 GND A34	FRAME#
B35 IRDY# A35	GND
B36 +V3.3 A36	TRDY#
B37 DEVSEL# A37	GND
B38 GND A38	STOP#
B39 LOCK# A39	+V3.3
B40 PERR# A40	SMBCLK
B41 +V3.3 A41	SMBDATA
B42 SERR# A42	GND
B43 +V3.3 A43	PAR
B44 CBE#1 A44	AD15
B45 AD14 A45	+V3.3
B46 GND A46	AD13
B47 AD12 A47	AD11
B48 AD10 A48	GND
B49 GND A49	AD9
B52 AD8 A52	CBE#0
B53 AD7 A53	+V3.3
B54 +V3.3 A54	AD6
B55 AD5 A55	AD4
B56 AD3 A56	GND
B57 GND A57	AD2
B58 AD1 A58	AD0
B59 +V5 A59	+V5
B60 ACK64# A60	#PCI1_REQ64
B61 +V5 A61	+V5
B62 +V5 A62	+V5

B.51 PCI Slot (PCI2)



Pin	Signal	Pin	Signal
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	NC	A4	TDI
B5	+5V	A5	+V5
B6	+5V	A6	INT#D
B7	INT#A	A7	INT#B
B8	INT#C	A8	+V5
B9	NC	A9	NC
B10	NC	A10	+V5
B11	NC	A11	NC
B12	GND	A12	GND
B13	GND	A13	GND
B14	NC	A14	+V3.3_DUAL
B15	GND	A15	RST#
B16	CLK33M_PCI	A16	+V5
B17	GND	A17	GNT#3
B18	PCI_REQ#3	A18	GND
B19	+V5	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	+V3.3
B22	GND	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND
B25	+V3.3	A25	AD24
B26	PCI_CBE#3	A26	AD19
B27	AD23	A27	+V3.3
B28	GND	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	GND
B31	+V3.3	A31	AD18
B32	AD17	A32	AD16
B33	PCI_CBE#2	A33	+V3.3
B34	GND	A34	FRAME#
B35	IRDY#	A35	GND
B36	+V3.3	A36	TRDY#
B37	DEVSEL#	A37	GND
B38	GND	A38	STOP#
			·

B39	LOCK#	A39	+V3.3
B40	PERR#	A40	SMBCLK
B41	+V3.3	A41	SMBDATA
B42	SERR#	A42	GND
B43	+V3.3	A43	PAR
B44	CBE#1	A44	AD15
B45	AD14	A45	+V3.3
B46	GND	A46	AD13
B47	AD12	A47	AD11
B48	AD10	A48	GND
B49	GND	A49	AD9
B52	AD8	A52	CBE#0
B53	AD7	A53	+V3.3
B54	+V3.3	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	GND
B57	GND	A57	AD2
B58	AD1	A58	AD0
B59	+V5	A59	+V5
B60	ACK64#	A60	#PCI1_REQ64
B61	+V5	A61	+V5
B62	+V5	A62	+V5
-			

B.52 COM78910 Setting Pin Header (JSETCOM7)



Pin	Signal	Pin	Signal
1	UART_SIN [7]	2	RXD_RS485
3	UART_SIN [7]	4	RXD_RS422
5	UART_SIN [7]	6	RXD_RS232
7	DCDA	8	SOUT [7]
9	COM7_DCD#	10	COM7_SOUT
11	COM7_TXD485-	12	COM7_RXD485+
13	SIN [7]	14	DTR [7]
15	COM7_SIN	16	COM7_DTR#
17	COM7_TXD485+	18	COM7_RXD485-

B.53 LVDS/eDP Backlight Inverter Power Header (INV1)



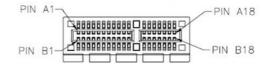
Pin	Signal
1	+12V
Inv12	GND
3	BKL EN
4	BKL CTRL
5	+5V

B.54 LVDS Panel Voltage Selection Header (JLVDS1)



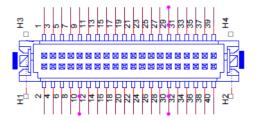
Pin	Signal	Pin	Signal
1	NC	2	+5V
3	+12V	4	EDP1 VDD
5	NC	6	+3.3V

B.55 PCIe x1 Slot (PCIEX1_1)



Pin	Signal	Pin	Signal
B1	+12V	A1	PRSNT1#
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	Reserved
B6	SMB_DATA	A6	Reserved
B7	GND	A7	Reserved
B8	+3.3V	A8	Reserved
B9	Reserved	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	WAKE#	A11	PWRGD
B12	Reserved	A12	GND
B13	GND	A13	REFCLK+
B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	PRSNT2#	A17	RX0-
B18	GND	A18	GND

B.56 LVDS/eDP Panel Header (LVDS_EDP1)



For LVDS(Low-voltage differential signaling interface)

Pin	Signal	Pin	Signal
1	VDD	21	A2P(EDP_CPU_TXP0)
2	VDD	22	A6P
3	DET#	23	GND
4	GND	24	GND
5	VDD	25	CLK1N(EDP_CPU_TXN3)
6	VDD	26	CLK2N
7	A0N(EDP_CPU_TXN2)	27	CLK1P(EDP_CPU_TXP3)
8	A4N	28	CLK2P
9	A0P(EDP_CPU_TXP2)	29	GND
10	A4P	30	GND
11	GND	31	SCD
12	GND	32	SDD
13	A1N(EDP_CPU_TXN1)	33	GND
14	A5N	34	GND(EDP_CH7511_HPD)
15	A1P(EDP_CPU_TXP1)	35	A3N
16	A5P	36	A7N
17	GND	37	A3P
18	GND	38	A7P
19	A2N(EDP_CPU_TXN0)	39	ENBKL
20	A6N	40	VCON

For eDP(Embedded displayport)

Pin	Signal	Pin	Signal
1	VDD	21	A2P(EDP_CPU_TXP0)
2	VDD	22	NC
3	NC	23	GND
4	GND	24	GND
5	VDD	25	CLK1N(EDP_CPU_TXN3)
6	VDD	26	NC
7	A0N(EDP_CPU_TXN	12) 27	CLK1P(EDP_CPU_TXP3)
8	A4N	28	NC
9	A0P(EDP_CPU_TXP	2) 29	GND
10	A4P	30	GND

GND	31	SCD (EDP_AUX+)
GND	32	SDD (EDP_AUX-)
A1N(EDP_CPU_TXN1)	33	GND
A5N	34	GND(EDP_CH7511_HPD)
A1P(EDP_CPU_TXP1)	35	NC
A5P	36	NC
GND	37	NC
GND	38	NC
A2N(EDP_CPU_TXN0)	39	NC
NC	40	NC
	GND A1N(EDP_CPU_TXN1) A5N A1P(EDP_CPU_TXP1) A5P GND GND A2N(EDP_CPU_TXN0)	GND 32 A1N(EDP_CPU_TXN1) 33 A5N 34 A1P(EDP_CPU_TXP1) 35 A5P 36 GND 37 GND 38 A2N(EDP_CPU_TXN0) 39

B.57 LVDS VESA, JEIDA Format Selection Pin Header (JLVDS_VCON1)



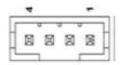
Pin	Signal
1	+3.3V
3	OPTION
5	GND

B.58 SPDIF Pin Header (SPDIF1)



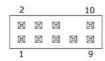
Pin	Signal
1	+5V
2	KEY
3	SPDIF OUT
4	GND

B.59 Audio Amplifier Pin Header (AMP1)



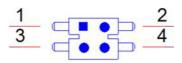
Pin	Signal
1	R+
2	GND
3	GND
4	L+

B.60 Front Audio Pin Header (FPAUD1)



Pin	Signal	Pin	Signal
1	MIC IN-L	2	GND
3	MIC IN-R	4	FPAUD_DETECT#
5	LINE OUT-R	6	SENSE R1
7	SENSE	8	KEY
9	LINE OUT-L	10	SENSE R2

B.61 LAN Active LED Pin Header (LANLED1)



Pin	Signal	Pin	Signal
1	LAN1_ACT#	2	LAN2 _ACT#
3	LAN LED PWR	4	LAN LED PWR

B.62 COM1 RI# Selection Pin Header(JSETCOM1_V1)



Pin	Signal	Pin	Signal
1	RI# [1]	2	Advantech define
3	Advantech define	4	+5V
5	+12V	6	Advantech define

B.63 COM2 RI# Selection Pin Header(JSETCOM2_V2)



Pin	Signal	Pin	Signal
1	RI# [2]	2	Advantech define
3	Advantech define	4	+5V
5	+12V	6	Advantech define



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